APOGEE TECHNOLOGY, INC.

DDXi-2051

2.0/2.1 Channel Integrated Audio Controller and Power Output

FEATURES

- **3 Power Output Configurations**
- **DDX® Mono-Mode:**
  - o 1 x 80 W 4Ω < 10% THD
- **DDX Full-Bridge Mode:**
  - o 2 x 40 W 8Ω < 10% THD
- **2.1 Channel Mode:**
  - o 2 x 20 W 4Ω +1 x 40 W 8Ω < 10% THD
- **Power SO-36 Package**
- **2.0 / 2.1 Channels of 24-Bit DDX®**
- **100dB SNR and Dynamic Range**
- **32kHz to 192kHz Input Sample Rates**
- **Digital Gain/Attenuation +48dB to –80dB in 0.5dB steps**
- **Four (4) 24-bit Programmable Biquads (EQ) per Channel**
- **I²C Control**
- **2-Channel I²S Input Data Interface**
- **Each Channel and Master Gain/Attenuation, Soft and Hard Mute**
- **Individual Channel Volume and EQ Bypass**
- **Bass/Treble Tone Control**
- **Dual Independent Programmable Limiters/Compressors**
- **Automodes™**
  - *** 31 Preset EQ Curves**
  - *** 15 Preset Crossover Settings**
  - *** Auto Volume Controlled Loudness**
  - *** 3 Preset Volume Curves**
  - *** 2 Preset Anti-Clipping Modes**
  - *** Preset Night-time Listening Mode**
- **Input and Output Channel Mapping**
- **AM Noise Reduction and PWM Frequency Shifting Modes**
- **Soft Volume Update and Muting**
- **Auto Zero and Invalid Input Detect Muting**
- **Selectable DDX® Ternary or Binary PWM output + Variable PWM Speeds**
- **Selectable De-emphasis**
- **Post-EQ User Programmable Mix with default 2.1 Bass Management settings**
- **Variable Max Power Correction for lower full-power THD**
- **Over-current and Over-Temperature protection with programmable recovery**
- **Thermal-Warning Indicator with programmable auto output power reduction**
- **Four (4) Output Routing Configurations**
- **24-bit, 96kHz Internal Processing**
- **BBE or BBE+Viva Processing***
  ***Provided only under license from BBE Sound, Inc.**
- **QXpander****
  *** *Provided only under License of QSound Labs, Inc.**

1.0 GENERAL DESCRIPTION

The DDXi-2051 is the world's first integrated solution including digital audio processing, digital amplifier control, and high-power output in a single DDX® chip delivering high-quality, high-efficiency, all digital amplification in a single compact package.

The DDXi-2051 can be configured via digital control to operate in several output modes providing up to 2.1 channels of power output to speakers. The device is capable of delivering up to 2 x 20W + 1 x 40W in 2.1 mode or 2 x 40W in stereo mode. It can also be configured as a single bridge capable of high-current operation delivering up to 1 x 80W.

The DDXi-2051 boasts a full assortment of audio signal processing features that includes up to 4 programmable 24-bit biquads (EQ) per channel and bass/treble tone control. Automodes™ enable a time-to-market advantage by substantially reducing the amount of software development needed for certain functions. AutoMode settings include Auto Volume loudness control, preset volume curves, preset EQ settings, new advanced AM radio interference reduction modes, and more.

The serial audio data input interface accepts most formats, including the popular I²S format. Three channels of DDX® processing are provided. This high quality conversion from PCM audio to DDX's patented tri-state PWM switching waveform provides up to 100dB SNR and dynamic range.

Specifications are subject to change without notice.

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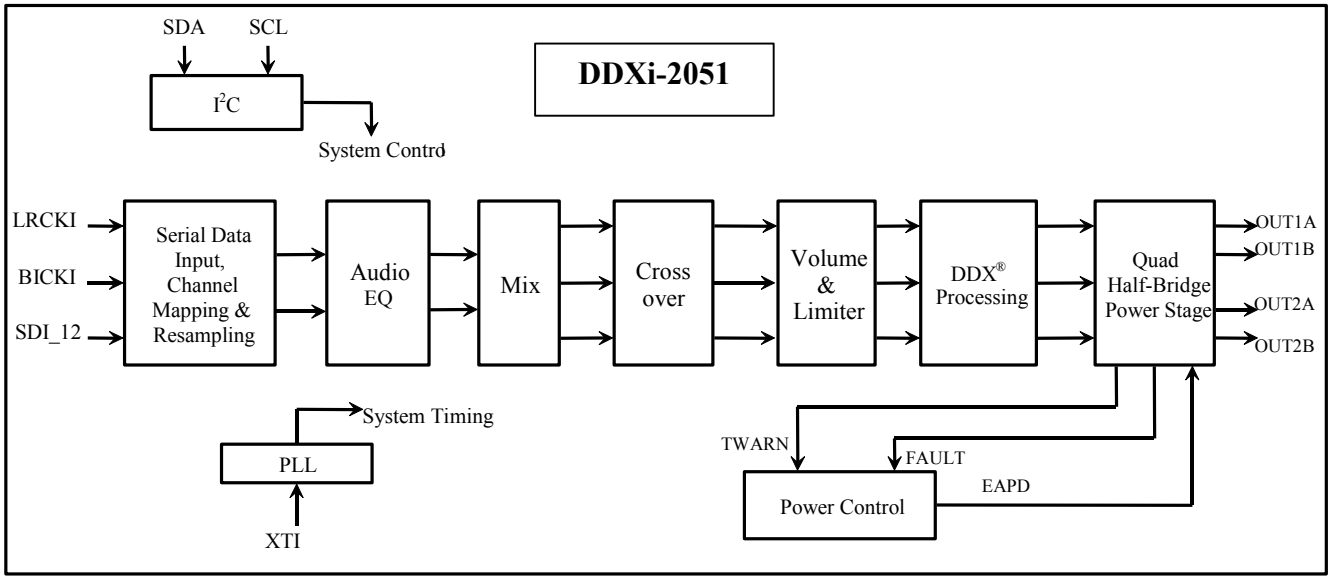


Figure 1 - Block Diagram

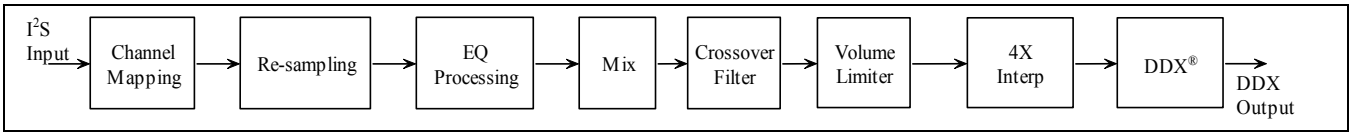


Figure 2 - Channel Signal Flow Diagram through the Digital Core

1.1 EQ Processing

Two channels of re-sampled input data (96 kHz) are provided as input to the EQ processing block. Figure 3 below shows the internal signal flow through the EQ block. In this block, up to 4 user-defined Biquads can be applied to each of the two main processing channels. Pre-scaling, dc-blocking high-pass, de-emphasis, bass, and tone control filters can also be applied based on various configuration parameter settings. The entire EQ block can be bypassed for all channels simultaneously by setting the DSPB bit to '1'. The CxEQBP bits can be used to bypass the EQ block on a per channel basis.

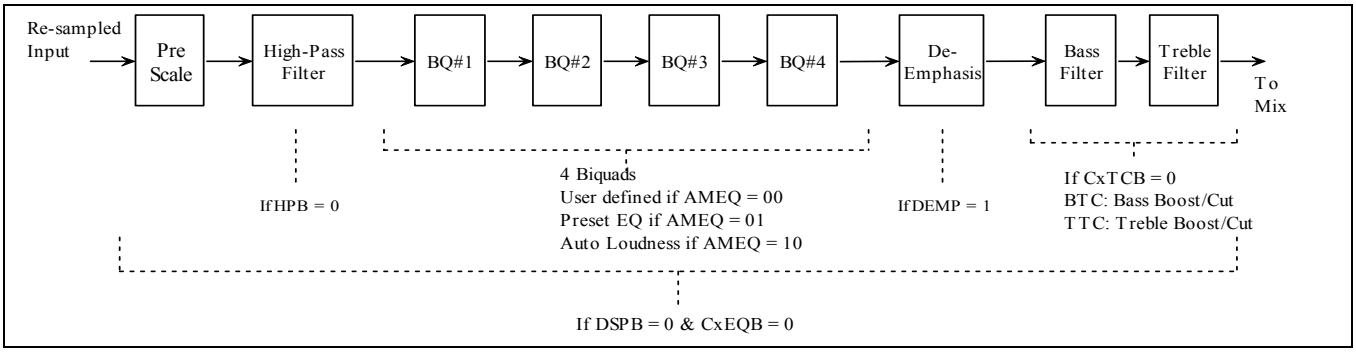


Figure 3 - Channel Signal Flow through the EQ Block

1.2 Mix Processing

The Post-EQ Mix block takes the two channel outputs from the EQ block and outputs three channels of data. By default, Channels 1 and 2 outputs are essentially pass-through of Channels 1 and 2 inputs coming from the EQ block. An additional channel is created as a result of a sum & mix of the two input channels. See Figure 26. By default, this 3rd channel of data is an equal mix of channel 1 and 2 data. Normally this third channel will be used as the subwoofer in a 2.1 configuration. An additional filtering stage is found after the mix block in order to implement crossover filtering. The crossover filters can be automatically configured from the AutoMode Crossover (XO) bits or these filters can be manually programmed for any type and frequency crossover.

1.3 Output Mode Configurations

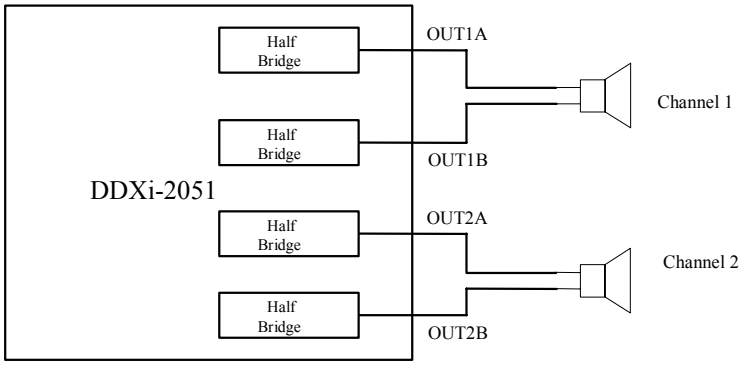


Figure 4 - 2-Channel (Full-bridge) Power, OCFG(1…0) = 00

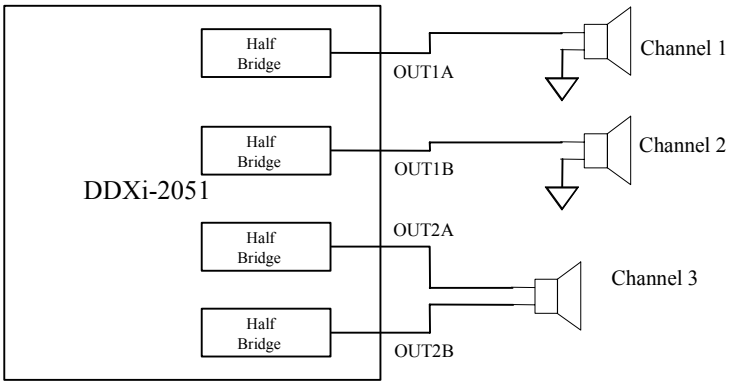


Figure 5 - 2.1-Channel Power Configuration OCFG(1…0) = 01

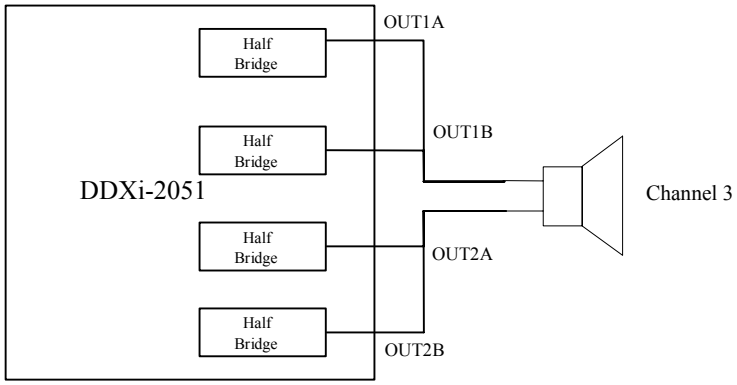


Figure 6 - Mono-Parallel Configuration, OCFG(1…0) = 11

2.0 PIN FUNCTION AND SPECIFICATIONS

2.1 Pin Description and Numbering

Table 1 - Pin Description and Numbering

Pin Name	Pin No.	Description	
Input and Clock Interface			
SCL	23	I^2C Serial Clock, 5V Tolerant Schmitt Trig Input.	
SDA	24	I^2C Serial Data, bdir, 5V Tolerant Schmitt Trig Input and 3.3V, 2mA Output.	
XTI	27	PLL Clock, 5V Tolerant Input.	
SDI_12	30	I^2S Serial Data Channels 1 & 2, 5V Tolerant Schmitt Trig Input.	
LRCKI	31	I^2S Left/Right Frame Sync Clock, 5V Tolerant Input.	
BICKI	32	I^2S Serial Bit Sync Clock, 5V Tolerant Input.	
Control/Miscellaneous			
CONFIG	21	Logic Levels.	
RESET	22	Reset (0=Reset, 1= Normal), 5V Tolerant Schmitt Trig Input.	
GND	25	Connect to ground.	
PLL_FILTER	26	Connection to PLL Filter. Refer to application schematic for PLL Filter details.	
NC	1,2,5,14	Do not connect.	
Power Outputs:		**DDX® Mode**	**Binary 2.1 Channel Mode**
OUT1A	16	Channel 1 Positive output.	Channel 1 output.
OUT1B	10	Channel 1 Negative output.	Channel 2 output.
OUT2A	9	Channel 2 Positive output.	Channel 3 Positive output.
OUT2B	3	Channel 2 Negative output.	Channel 3 Negative output.
Power Supplies			
VCC [2B, 2A, 1B, 1A]	4, 8, 11, 15	Power Positive Supply	
GND [2B, 2A, 1B, 1A]	6, 7, 12, 13	Power ground	
GNDCLEAN	17	Logic reference ground.	
GNDSUB	18	Substrate ground.	
VREG1	19	Internal +5V Regulator Voltage	
VDD3	20	Logic Supply to Power Section	
GNDA	28	PLL Analog Ground	
VDDA	29	PLL Analog Supply (3.3V)	
GND3	33	Digital Ground	
VDD3	34	Digital Power Supply Voltage (3.3V)	
VREG2	35	Internal -5V (relative to VSIG) Regulator Voltage	
VSIG	36	Signal Positive Supply	

2.2 Absolute Maximum Ratings [Note 1]

Symbol	Parameter	Value	Unit
$V_{DD\ 3.3}$	3.3V Digital Power Supply	-0.5 to 4	V
V_{DDA}	3.3V Analog Power Supply	-0.5 to 4	V
V_i	Voltage on input pins	-0.5 to (Vdd + 0.5)	V
V_o	Voltage on output pins	-0.5 to (Vdd + 0.5)	V
V_b	Voltage on 5V tolerant inputs and bi-directional pins [Note 2]	-0.5 to 5.5	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_j	Operating Junction Temperature Range	0 to +150	°C
V_{CC}	Power supply voltage	40	V
V_L	Input logic reference	5.5	V

Note 1 - Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2 - Withstands -0.8V undershoot and 6.3V overshoots for 4ns max.

2.3 Thermal Data

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
P_{TOT}	Power Dissipation, $T_{heat\text{-}spreader}$ = 25°C			40	W
$\theta_{J\text{-}C}$	Thermal resistance junction-case (heat spreader)			3.0	°C/W
$T_{j\text{-}SD}$	Thermal shut-down junction temperature		150		°C
T_{WARN}	Thermal warning temperature		130		°C
T_{hSD}	Thermal shut-down hysteresis		25		°C

2.4 Electrical Characteristics.

(Unless otherwise noted, V_{CC} = 26V, V_{DD3} = 3.3V, T_c = 25°C, R_L = 8Ω.)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$P_{O\text{-}DM}$ (DDX Mono Mode)	Power Per Channel	THD+N <10%, R_L=4Ω, V_{CC} = 27V	80			W_{RMS}
		THD+N <1%, R_L=4Ω, V_{CC} = 27V	62			
$P_{O\text{-}DF}$ (DDX Full Bridge Mode)	Power Per Channel	THD+N <10%, R_L=8Ω	40			W_{RMS}
		THD+N <1%, R_L=8Ω	30			
$P_{O\text{-}Bin}$ (2.1 Channel Mode)	Power Per Channel, 1 x Full-Bridge	THD+N <10%, R_L=4Ω,	40			W_{RMS}
		THD+N <1%, R_L=4Ω	30			
	Power Per Channel, 2 x Half Bridge	THD+N <10%, R_L=4Ω	20			
		THD+N <1%, R_L=4Ω	15			
THD+N	Total Harmonic Distortion + Noise	DDX Stereo Mode, Po=1 Wrms		0.05		%
		DDX Stereo Mode, Po=26Wrms		0.10		
SNR	Signal to Noise Ratio, DDX® Modes	A-Weighted (NSBW = 1)		100		dB
	Signal to Noise Ratio, Binary Modes	A-Weighted (NSBW = 1)		90		
PSRR	Power Supply Rejection Ratio	Stereo DDX Mode, < 5 kHz V_{RIPPLE}=1 V_{RMS} Audio Input = Dither Only		80		dB
X_{TALK}	Crosstalk	Stereo DDX Mode, < 5 kHz One Channel Driven @ 1 W Other Channel Measured		80		dB
η	Peak Efficiency, DDX® Mode	Po=2 x 40 W, 8Ω		89		%
	Peak Efficiency, Binary Modes	Po=2 x 20 W, 4Ω + 1 x 40W, 8Ω		87		
I_{SC}	Speaker Output Short-Circuit Protection Limit per Bridge		3	6	8	A
$R_{ds\text{-}on}$	Power MOSFET output resistance	I_d=1A		200	270	mΩ
g_N	Power Nchannel $R_{ds\text{-}on}$ matching	I_d = 1A	95			%
I_{dss}	Power Pchannel/Nchannel leakage	V_{CC} = 35 V			50	uA
UVL	Under-voltage Lockout Threshold			7	9	V
I_{PD}	V_{CC} supply current, Power-down	Soft-Pwdn or EAPD = 0		<1		mA

2.4 Electrical Characteristics.

(Unless otherwise noted, V_{CC} = 26V, V_{DD3} = 3.3V, T_c = 25°C, R_L = 8Ω.)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{CC}	2-channel mode V_{CC} supply current	2-Channel switching at 384kHz.		75		mA
	2.1-channel mode V_{CC} supply current	2.1-Channel switching at 384kHz		84		
t_r	Rise time	Resistive load			25	ns
t_f	Fall Time	Resistive load			25	ns

2.5 Operating Conditions

2.5.1 Recommended DC Operating Conditions [Note 3]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Power supply voltage	9		36	V
V_{DD3}	3.3V Digital Power Supply Voltage	3.0		3.6	V
V_{DDA}	3.3V Analog Power Supply	3.0		3.6	V
T_A	Operating Ambient Temperature	0		70	°C

Note 3 - Performance not guaranteed beyond recommended operating conditions.

2.5.2 DC Electrical Characteristics: 5V Tolerant Input Buffers

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{ILhyst}	Low Level Threshold	Input Falling	0.8		1.35	V
V_{IHhyst}	High Level Threshold	Input Rising	1.3		2.0	
V_{hyst}	Schmitt Trigger Hysteresis		0.3		0.8	V
I_{IL}	Low Level Input Current	Vi = 0V [*Note 4*]	40	60	110	uA
I_{IH}	High Level Input Current	Vi = VDD_3.3 [*Note 4*]	25	60	110	uA

Note 4 - Min condition: Vdd=3V, 125°C; Max condition: Vdd=3.6V, -40°C.

2.5.3 Operating Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{VDD}	Operating Current 3.3V	All channels operating		6	8	mA
	PowerDown Current 3.3V	PowerDown Asserted		2	3	mA
I_{VDDA}	PLL Operating Current 3.3V			9	12	MA
	PLL PowerDown Current 3.3V	PowerDown Asserted		2	3	mA

2.5.4 Electrical Characteristics

(V_{DD3}= 3.3 ± 0.3V, TA=0 to 70°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{ESD}	Electrostatic Protection	Leakage <1uA (Note 5)	2000			V

Note 5 - Human Body Model.

2.5.5 Timing Characteristics

(V_{DD3}= 3.3 ± 0.3V, T_A=0 to 70°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{reset}	Reset hold time	Active Low Reset (pin 15)	100			nSec
VCO Free_Run	VCO Free Run Frequency	No Clock applied to XTI	18	28		MHz

Note 6 - The DDXi-2051 is designed to operate at a minimum free-run frequency when there is no clock applied at XTI. This assures proper I^2C communication without a valid master clock. The device is not designed to process audio data without a valid clock applied at XTI.

3.0 FUNCTIONAL DESCRIPTION

3.1 Pin Functional Description

3.1.1 OUT1A, 1B, 2A & 2B (Pins 16, 10, 9 & 3)

Half Bridge Power Outputs 1A, 1B, 2A & 2B deliver audio power to the speaker loads. Using DDX stereo configuration mode, outputs 1A (+) and 1B (-) comprise Channel 1 and outputs 2A (+) and 2B (-) comprise Channel 2. Using binary 2.1 channel configuration mode, output 1A is for Channel 1 and output 1B is for Channel 2 and outputs 2A (+) and 2B (-) comprise Channel 3. Using DDX mono-high power output mode (Config connected to VREG1), outputs 1A and 1B are shorted (+) and outputs 2A and 2B are shorted (-) comprising a single BTL output with double the output current capability for Channel 3. Operation as four individual half-bridges is not supported.

3.1.2 RESET (Pin 22)

Driving RESET low sets all outputs low and returns all register settings to their defaults. The reset is asynchronous to the internal clock.

3.1.3 I^2C Signals (Pins 23 & 24)

The SDA (I^2C Serial Data) and SCL (I^2C Serial Clock) pins operate per the I^2C specification. (See Section 4.0). Fast-mode (400kB/sec) I^2C communication is supported.

3.1.4 GNDA & VDDA: Phase Locked Loop Power (Pins 28-29)

The phase locked loop power is applied here. This +3.3V supply must be well bypassed and filtered for noise immunity. The audio performance of the device is critically dependent upon the PLL circuit. Refer to application schematics for suggested filtering.

3.1.5 XTI: PLL Clock In (Pin 27)

The master clock applied on this pin for the PLL is required for the operation of the digital core. The master clock must be an integer multiple of the LR clock frequency. Typically, the master clock frequency is 12.288 MHz (256*Fs) for a 48kHz sample rate, which is the default at power-up. Care must be taken to avoid over-clocking the device, i.e provide the device with the nominally required system clock; otherwise, the device may not properly operate or be able to communicate.

3.1.6 FILTER_PLL: PLL Filter (Pin 26)

This pin connects to external filter components for PLL loop compensation. Refer to the application schematics for the recommended PLL loop compensation circuit.

3.1.7 BICKI: I^2S Serial Clock In (Pin 32)

The serial or bit clock input is used for framing each data bit. The bit clock frequency is typically 64*Fs, for example, using I^2S serial format.

3.1.8 SDI_12: I^2S Serial Data Input (Pin 30)

PCM audio information enters the device here. Six format choices are available including I^2S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20, and 24 bits.

3.1.9 LRCKI: I^2S Left/Right Clock In (Pin 31)

The Left/Right clock input is used for data word framing. The clock frequency will be at the input sample rate Fs.

3.1.10 CONFIG: Configuration input (Pin 21)

The configuration input pin is normally connected to ground. Using the mono-high power BTL configuration requires the CONFIG input pin be shorted to VREG1.

3.1.11 VREG1: Internal regulator bypass (Pin 19)

Connect a 100nF bypass capacitor to this pin to stabilize the internal +5V regulator in the power stage.

3.1.12 VREG2: Internal regulator bypass (Pin 35)

Connect a 100nF bypass capacitor between this pin and VSIG to stabilize the internal -5V regulator in the power stage. Note, VREG2 is measured relative to VSIG.

3.1.13 VSIG: Signal Positive Supply (Pin 36)

Connect a 100nF bypass capacitor to this pin to stabilize the reference for the upper regulator in the power stage.

3.1.14 GNDSUB: Substrate ground (Pin 18)

Connect this pin to power ground plane.

3.1.15 GNDCLEAN: Clean ground (Pin19)

This pin is the logic ground reference for the power section. Connect this pin to digital ground plane. Note, digital and power ground planes must be combined under the IC.

3.1.16 VCC1A,1B,2A,2B and GND1A,1B,2A,2B: Bridge Power Supply (Pins 15,11,8,4 and Pins 13,12,7,6)

These pins supply voltage to the power stage section using one power pair for each half bridge. It is absolutely critical to bypass well using low-inductance PCB routing for these power inputs. Apogee provides reference circuit/PCB designs to adopt for customer applications. It is strongly recommended to obtain these designs from application support and copy the application circuit/layout exactly.

3.1.17 VDD3 and GND3: Digital power supply (Pins 20,34 and 33).

Connect 100nF bypass capacitors very close to these supply pins.

3.2 Pin Connection (Top View)

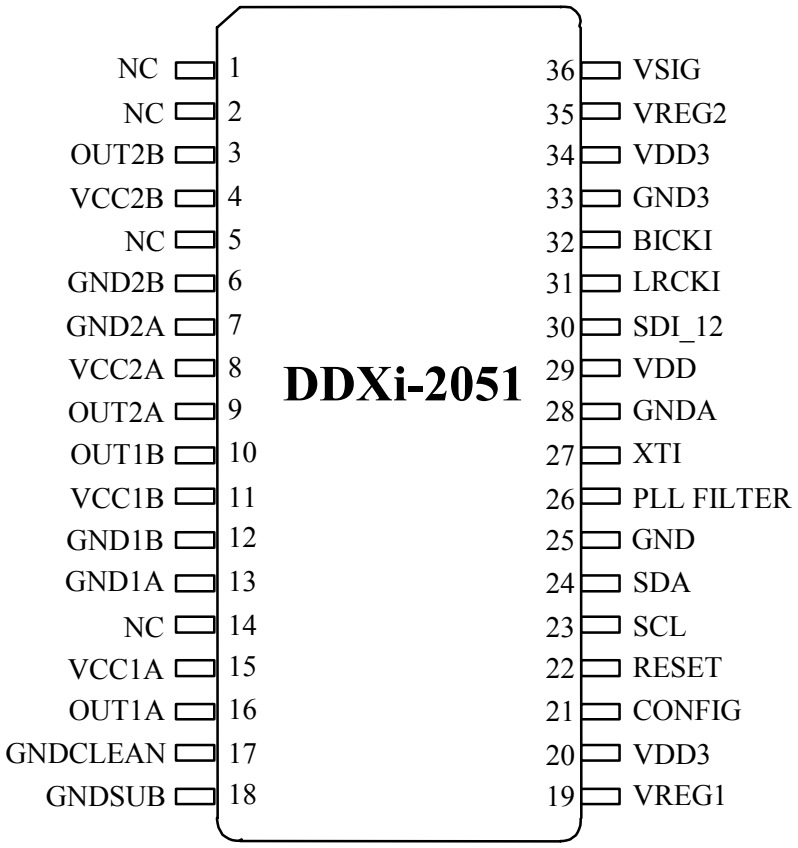


Figure 7 - Pin Connection Diagram.

3.3 Audio Performance

3.3.1 DDX Operation with Vcc = 26V, 8 Ohm load

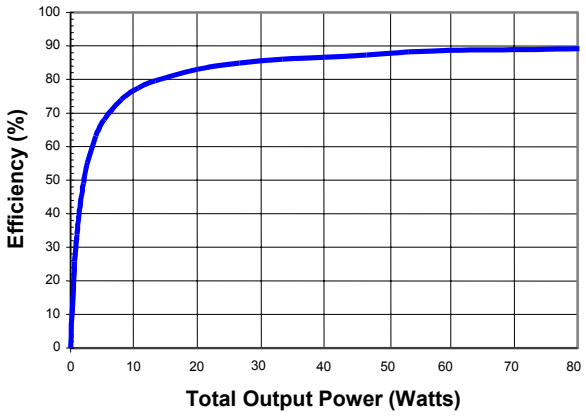


Figure 8 - Typical Efficiency

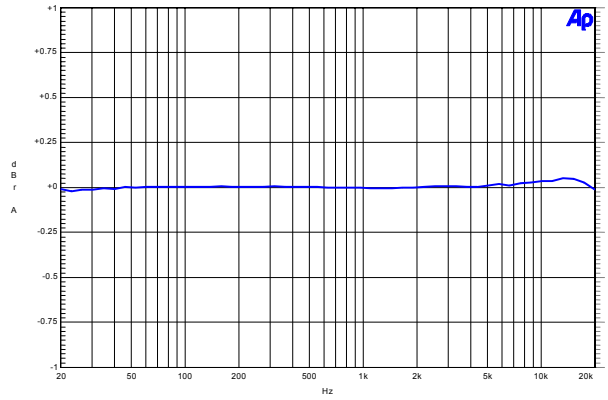


Figure 9 - Typical Frequency Response

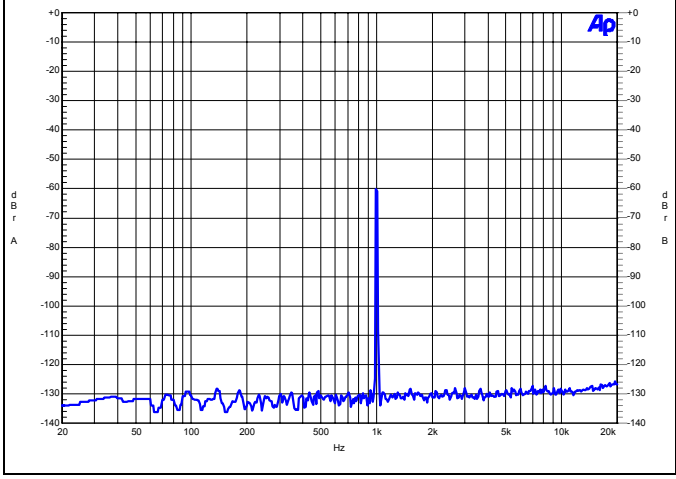


Figure 10 - FFT –60dB, 1kHz Output

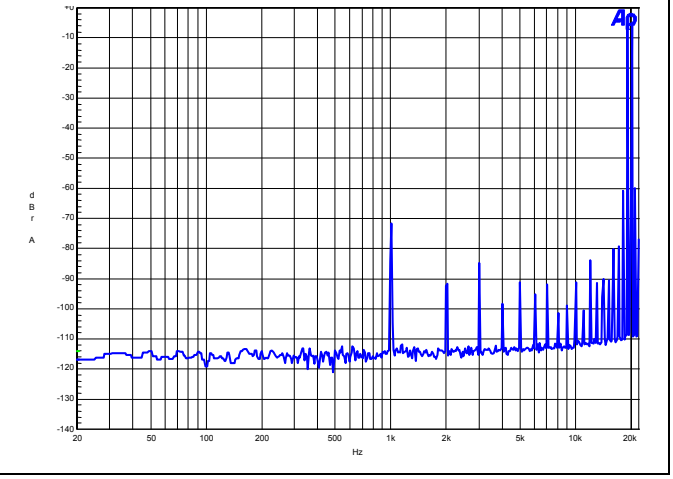


Figure 11 - FFT Inter-Modulation Distortion 19kHz and 20kHz

3.3.2 DDX Full Bridge Operation with Vcc = 26V, 8 Ohm load

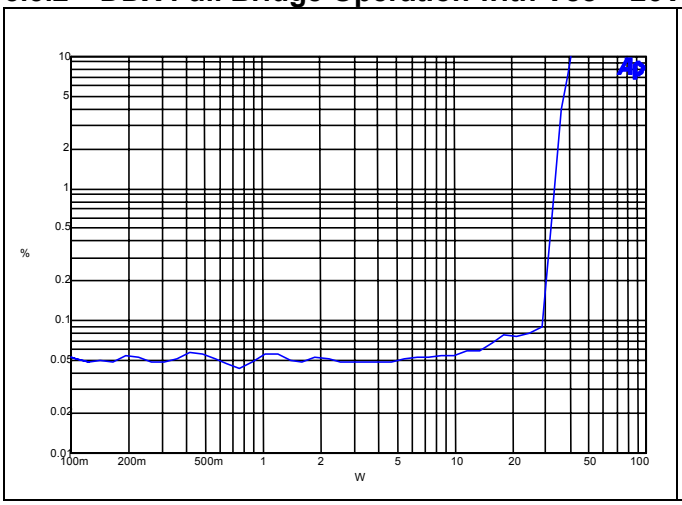


Figure 12 - THD vs. Power, 1kHz

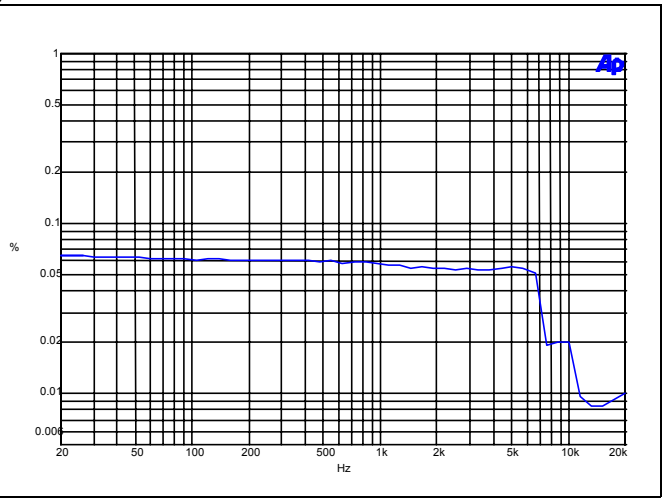


Figure 13 - THD vs. Frequency, 1W

3.3.3 DDX Full Bridge Operation with Vcc = 12V, 4 Ohm load

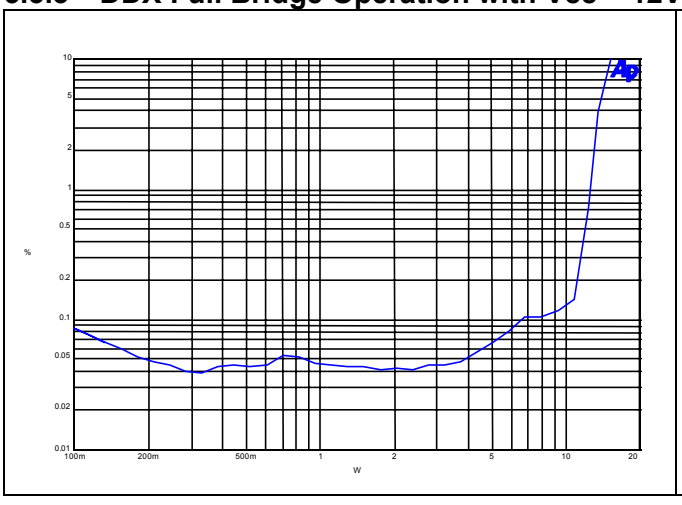


Figure 14 - THD vs. Power, 1kHz

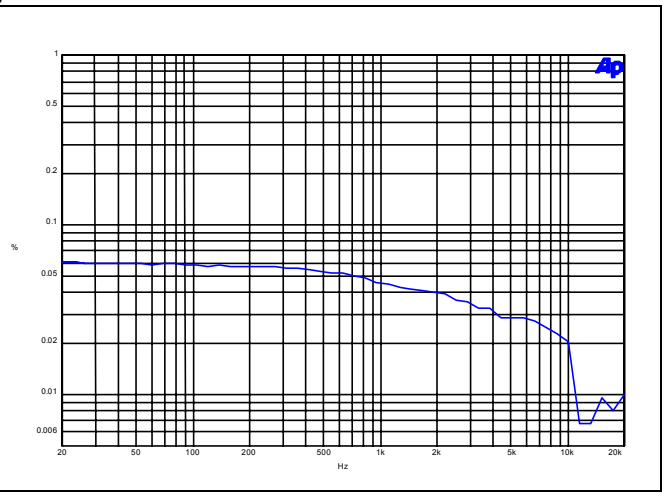


Figure 15 - THD vs. Frequency, 1W

3.3.4 DDX Mono Mode Operation with Vcc = 27V, 4 ohm load

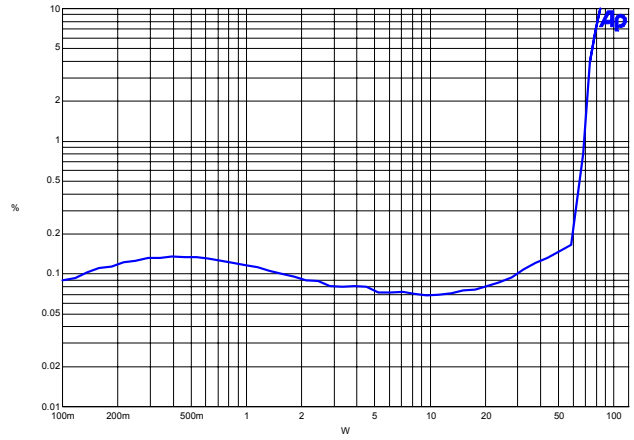


Figure 16 - THD vs. Power, 1kHz

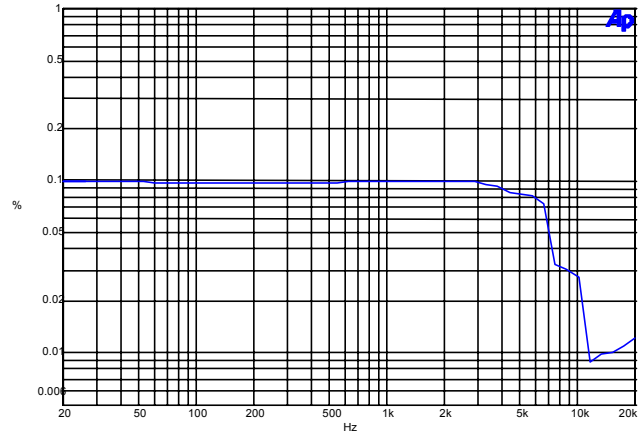


Figure 17 - THD vs. Frequency, 1W

3.3.5 Binary Half Bridge Operation with Vcc = 26V, 4 Ohm load

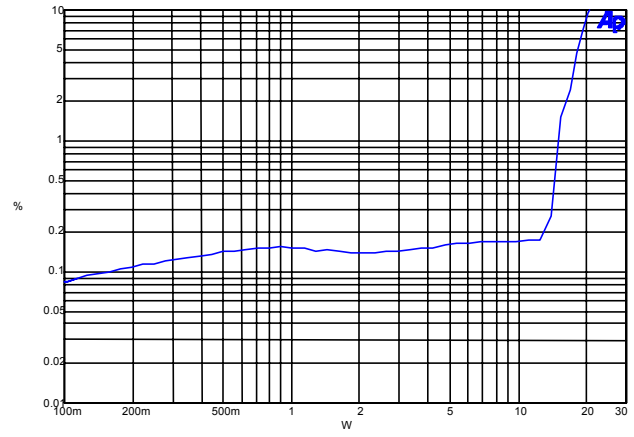


Figure 18 - THD vs. Power, 1kHz

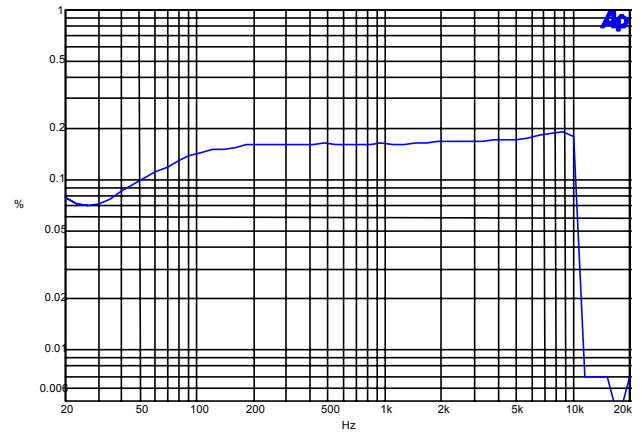


Figure 19 - THD vs. Frequency, 1W

4.0 I²C BUS SPECIFICATION

The DDXi-2051 supports the I²C fast mode (400 kb/sec) protocol. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The DDXi-2051 is always a slave device in all of its communications.

4.1 I²C Communication Protocol

4.1.1 Data Transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

4.1.2 Start Condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

4.1.3 Stop Condition

STOP is identified by a low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the DDXi-2051 and the bus master.

4.1.4 Data Input

During the data input the DDXi-2051 samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

4.2 Device Addressing

To start communication between the master and the DDXi-2051, the master must initiate with a start condition. Following this, the master sends 8-bits (MSB first) onto the SDA line corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the DDXi-2051 the I²C interface uses a device address of 0x34 or 0011010x.

The 8th bit (LSB) identifies read or write operation, RW. This bit is set to 1 in read mode and 0 for write mode. After a START condition the DDXi-2051 identifies the device address on the bus. If a match is found, it acknowledges the identification on the SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

4.3 Write Operation

Following the START condition the master sends a device select code with the RW bit set to 0. The DDXi-2051 acknowledges this and then the master writes the internal address byte. After receiving the internal byte address the DDXi-2051 again responds with an acknowledgement.

4.3.1 Byte Write

In the byte write mode the master sends one data byte. This is acknowledged by the DDXi-2051. The master then terminates the transfer by generating a STOP condition.

4.3.2 Multi-byte Write

The multi-byte write modes can start from any internal address. Sequential data byte writes will be written to sequential addresses within the DDXi-2051. The master generating a STOP condition terminates the transfer.

4.4 Read Operation

4.4.1 Current Address Byte Read

Following the START condition the master sends a device select code with the RW bit set to 1. The DDXi-2051 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

4.4.1.1 Current Address Multi-byte Read

The multi-byte read modes can start from any internal address. Sequential data bytes will be read from sequential addresses within the DDXi-2051. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

4.4.2 Random Address Byte Read

Following the START condition the master sends a device select code with the RW bit set to 0. The DDXi-2051 acknowledges this and then the master writes the internal address byte. After receiving, the internal byte address the DDXi-2051 again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The DDXi-2051 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

4.4.2.1 Random Address Multi-byte Read

The multi-byte read modes could start from any internal address. Sequential data bytes will be read from sequential addresses within the DDXi-2051. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

Write Mode Sequence

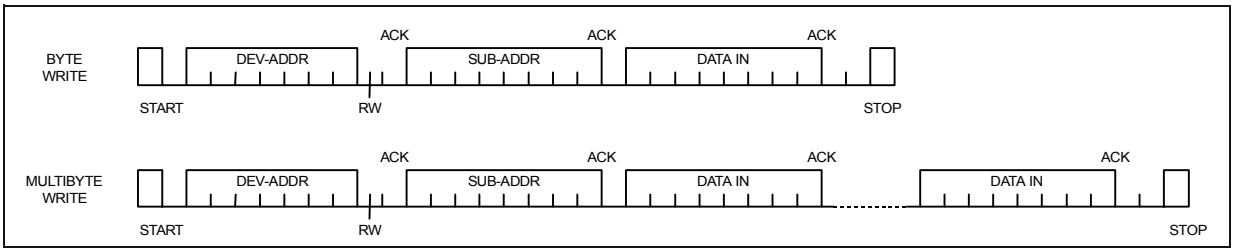


Figure 20 - I²C Write Procedure

Read Mode Sequence

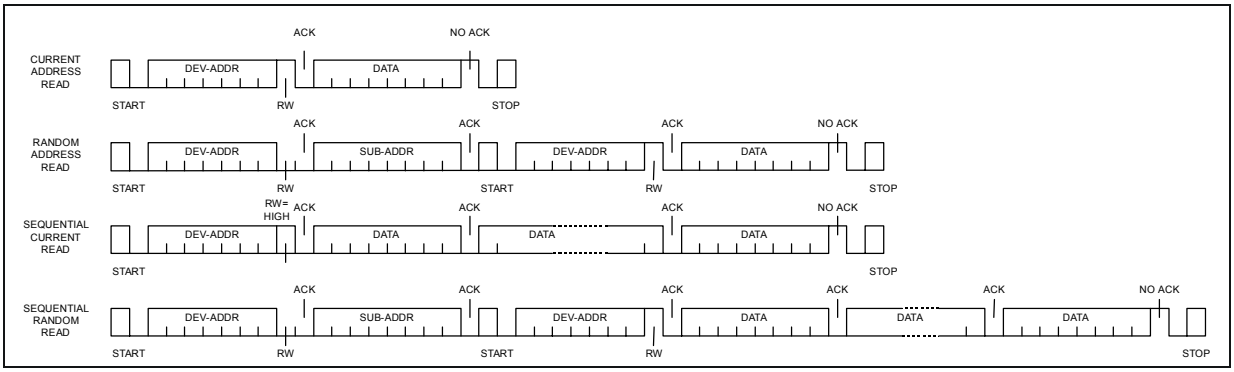


Figure 21 - I²C Read Procedure

Specifications are subject to change without notice.

5.0 REGISTER DESCRIPTION

Table 2 - I²C Register Summary

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	ConfA	FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0x01	ConfB	C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	ConfC		CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x03	ConfD	MME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0x04	ConfE	SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
0x05	ConfF	EAPD	PWDN	ECLE	LDTE	BCLE	IDE	OCFG1	OCFG0
0x06	Mmute					C3M	C2M	C1M	MMute
0x07	Mvol	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x08	C1Vol	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x09	C2Vol	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0A	C3Vol	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0B	Auto1	AMPS		AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0x0C	Auto2	XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0x0D	Auto3				PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
0x0E	C1Cfg	C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VBP	C1EQBP	C1TCB
0x1F	C2Cfg	C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VBP	C2EQBP	C2TCB
0x10	C3Cfg	C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VBP		
0x11	Tone	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0x12	L1ar	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x13	L1atrt	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x14	L2ar	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x15	L2atrt	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0x16	Cfaddr2	CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x17	B1cf1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x18	B1cf2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x19	B1cf3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x1A	B2cf1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x1B	B2cf2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x1C	B2cf3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x1D	A1cf1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
0x1E	A1cf2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x1F	A1cf3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0x20	A2cf1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x21	A2cf2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x22	A2cf3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x23	B0cf1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x24	B0cf2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x25	B0cf3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x26	Cfud					RA	R1	WA	W1
0x27	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x28	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x29	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*
0x2A	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*	*RES*
0x2B	FDRC1	FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0x2C	FDRC2	FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0x2D	Status	PLLUL						FAULT	TWARN

5.1 Configuration Register A (Address 00h)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	TWAB	TFRB	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	0	1	1

5.1.1 Master Clock Select

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	1	MCS0	Master Clock Select: Selects the ratio between the input I^2S sample frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	0	MCS2	

The DDXi-2051 will support sample rates of 32kHz, 44.1kHz, 48Khz, 88.2kHz, and 96kHz. The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency (fs). The correlation between the input clock and the input sample rate is determined by the status of the MCSx bits and the IR (Input Rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally.

Table 3 - IR and MCS Settings for Input Sample Rate and Clock Rate

Input Sample Rate fs (kHz)	IR	MCS (2...0)				
		1xx	011	010	001	000
32, 44.1, 48	00	128fs	256fs	384fs	512fs	768fs
88.2, 96	01	64fs	128fs	192fs	256fs	384fs
176.4, 192	10	64fs	128fs	192fs	256fs	384fs

5.1.2 Interpolation Ratio Select

BIT	R/W	RST	NAME	DESCRIPTION
4...3	R/W	00	IR (1...0)	Interpolation Ratio Select: Selects internal interpolation ratio based on input I^2S sample frequency

The DDXi-2051 has variable interpolation (re-sampling) settings such that internal processing and DDX output rates remain consistent. The first processing block interpolates by either 2 times or 1 time (pass-through) or provides a down-sample by a factor of 2. The IR bits determine the re-sampling ratio of this interpolation.

Table 4 - IR bit settings as a function of Input Sample Rate

Input Sample Rate Fs (kHz)	IR (1,0)	1st Stage Interpolation Ratio
32	00	2 times over-sampling
44.1	00	2 times over-sampling
48	00	2 times over-sampling
88.2	01	Pass-Through
96	01	Pass-Through
176.4	10	Down-sampling by 2
192	10	Down-sampling by 2

5.1.3 Thermal Warning Recovery Bypass

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	1	TWRB	Thermal-Warning Recovery Bypass: 0 – Thermal warning Recovery enabled 1 – Thermal warning Recovery disabled

If the Thermal Warning Adjustment is enabled (TWAB=0), then the Thermal Warning Recovery (TWRB=0) will remove the attenuation when the warning condition is de-asserted. If TWRB=1 and TWAB=0, when thermal warning is deasserted the Thermal Warning Adjustment will remain in effect until TWRB is changed to zero or the device is reset.

5.1.4 Thermal Warning Adjustment Bypass

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	1	TWAB	Thermal-Warning Adjustment Bypass: 0 – Thermal warning adjustment enabled 1 – Thermal warning adjustment disabled

The on-chip DDXi-2051 Power Output block provides feedback to the digital controller using inputs to the Power Control block. The TWARN input is used to indicate a thermal warning condition. When TWARN is asserted (set to 0) for a period greater than 400ms, the power control block will reduce the output level (default = -3dB) in an attempt to eliminate the thermal warning condition. The amount of attenuation under this condition can be controlled by the Thermal Warning – Post Scale value, which is located in the coefficient RAM, address 0x37. See Section 6.6 for modifying this value. After the thermal warning volume adjustment is applied, when TWARN is de-asserted the adjustment is removed if TWRB=0.

5.1.5 Fault Detect Recovery Bypass

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	FDRB	Fault-Detect Recovery Bypass: 0 – Fault Detect Recovery enabled 1 – Fault Detect Recovery disabled

The DDX Power block provides feedback to the digital controller using inputs to the Power Control block. The FAULT input is used to signal a fault condition (either over-current or thermal). When FAULT is asserted (set to 0), the power-block will be immediately disabled, the power control block will then attempt automatic recovery from the fault by asserting the tri-state signal in a sequence to reset the fault and retest the fault status. The sequence period, from fault to recovery attempt, can range from 0.1 milliseconds to 1 second as defined by the Fault-Detect Recovery Constant register (FDRC registers 29-2Ah). This sequence is repeated for as long as the fault condition exists. This feature is enabled by default but can be disabled by setting the FDRB control bit to 1. If Fault-Detect Recovery is disabled (not recommended), an output stage FAULT will cause a shut-down condition, which must be reset either by toggling the external reset pin or via a VCC power cycle to the IC.

5.2 Configuration Register B (Address 01h)

D7	D6	D5	D4	D3	D2	D1	D0
C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
1	0	0	0	0	0	0	0

5.2.1 Serial Audio Input Interface Format

BIT	R/W	RST	NAME	DESCRIPTION
3…0	R/W	0000	SAI (3...0)	Serial Audio Input Interface Format: Determines the interface format of the input serial digital audio interface.

Serial Data Interface

The DDXi-2051 serial audio input was designed to interface with standard digital audio components and to accept a number of serial data formats. The DDXi-2051 always acts as a slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using 3 input pins: left/right clock LRCKI (pin 33), serial clock BICKI (pin 31), and serial data 1 & 2 SDI12 (pin 32).

The SAI register (Configuration Register B – 01h, Bits D3-D0) and the SAIFB register (Configuration Register B – 01h, Bit D4) are used to specify the serial data format. The default serial data format is I^2S, MSB-First. Available formats are shown in Figure 22 and the tables that follow.

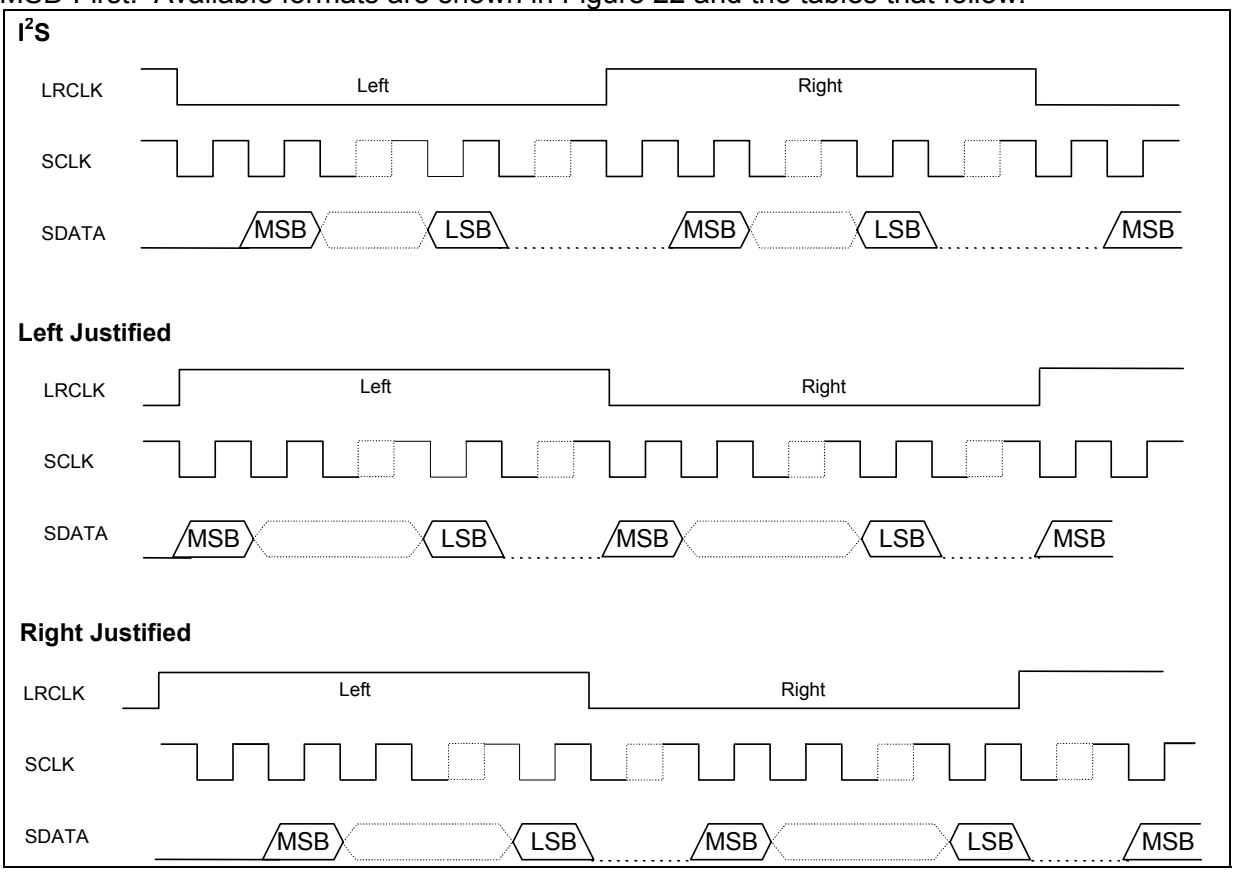


Figure 22 - Serial Audio Input and Output Formats

For example, SAI=1110 and SAIFB=1 would specify Right-Justified 16-bit data, LSB-First.

Table 6 below lists the serial audio input formats supported by the DDXi-2051 as related to BICKI = 32/48/64fs, where the sampling rate fs = 32/44.1/48/88.2/96/176.4/192 kHz.

Table 5 - First Bit Selection Table

SAIFB	Format
0	MSB-First
1	LSB-First

Note: Serial input and output formats are specified distinctly.

Table 6 - Supported Serial Audio Input Formats

BICKI	SAI (3...0)	SAIFB	Interface Format
32fs	1100	X	I^2S 15bit Data
	1110	X	Left/Right-Justified 16bit Data
48fs	0100	X	I^2S 23bit Data
	0100	X	I^2S 20bit Data
	1000	X	I^2S 18bit Data
	0100	0	MSB First I^2S 16bit Data
	1100	1	LSB First I^2S 16bit Data
	0001	X	Left-Justified 24bit Data
	0101	X	Left-Justified 20bit Data
	1001	X	Left-Justified 18bit Data
	1101	X	Left-Justified 16bit Data
	0010	X	Right-Justified 24bit Data
	0110	X	Right-Justified 20bit Data
	1010	X	Right-Justified 18bit Data
	1110	X	Right-Justified 16bit Data
64fs	0000	X	I^2S 24bit Data
	0100	X	I^2S 20bit Data
	1000	X	I^2S 18bit Data
	0000	0	MSB First I^2S 16bit Data
	1100	1	LSB First I^2S 16bit Data
	0001	X	Left-Justified 24bit Data
	0101	X	Left-Justified 20bit Data
	1001	X	Left-Justified 18bit Data
	1101	X	Left-Justified 16bit Data
	0010	X	Right-Justified 24bit Data
	0110	X	Right-Justified 20bit Data
	1010	X	Right-Justified 18bit Data
	1110	X	Right-Justified 16bit Data

Table 7 - Serial Input Data Timing characteristics (Fs = 32 to 192kHz)

BICKI FREQUENCY (slave mode)	12.5MHz max.
BICKI pulse width low (T0) (slave mode)	40 ns min.
BICKI pulse width high (T1) (slave mode)	40 ns min.
BICKI active to LRCKI edge delay (T2)	20 ns min.
BICKI active to LRCKI edge delay (T3)	20 ns min.
SDI valid to BICKI active setup (T4)	20 ns min.
BICKI active to SDI hold time (T5)	20 ns min.

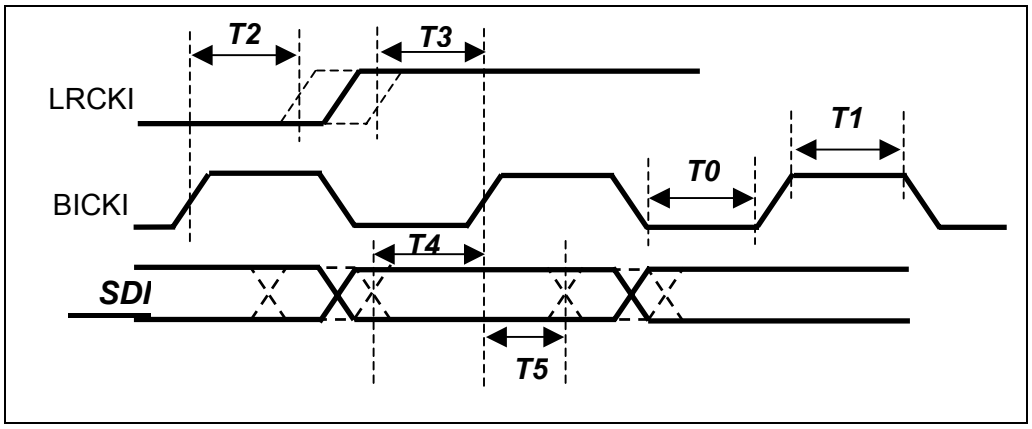


Figure 23 - Serial Input Data Timing Characteristics

5.2.2 Delay Serial Clock Enable

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	DSCKE	Delay Serial Clock Enable: 0 – No serial clock delay 1 – Serial clock delay by 1 core clock cycle to tolerate anomalies in some I2S master devices

5.2.3 Channel Input Mapping

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	0	C1IM	0 – Processing channel 1 receives Left I^2S Input 1 – Processing channel 1 receives Right I^2S Input
7	R/W	1	C2IM	0 – Processing channel 2 receives Left I^2S Input 1 – Processing channel 2 receives Right I^2S Input

Each channel received via I^2S can be mapped to any internal processing channel via the Channel Input Mapping registers. This allows for flexibility in processing. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

5.3 Configuration Register C (Address 02h)

D7	D6	D5	D4	D3	D2	D1	D0
	CSZ4	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
	1	0	0	0	0	1	0

5.3.1 DDX® Power Output Mode

BIT	R/W	RST	NAME	DESCRIPTION
1...0	R/W	10	OM (1...0)	DDX Power Output Mode: Selects configuration of DDX® output.

The DDX® Power Output Mode selects how the DDX® output timing is configured. The DDXi-2051's recommended use is OM = 10. When OM=11 the CSZ bits determine the size of the DDX® compensating pulse.

Table 8 - DDX® Output Modes

OM (1,0)	Output Stage – Mode
00	Not Used
01	Not Used
10	DDXi-2051
11	Variable Compensation

5.3.2 DDX® Variable Compensating Pulse Size

BIT	R/W	RST	NAME	DESCRIPTION
6...2	R/W	10000	CSZ (4...0)	Compensating Pulse Size Select

The DDX® variable compensating pulse size is not recommended to be used except in special circumstances . Contact Apogee applications for support when deciding to use this function.

Table 9 - DDX® Compensating Pulse

CSZ (4…0)	Compensating Pulse Size
00000	0 Clock period Compensating Pulse Size
00001	1 Clock period Compensating Pulse Size
…	…
10000	16 Clock period Compensating Pulse Size
…	…
11111	31 Clock period Compensating Pulse Size

5.4 Configuration Register D (Address 03h)

D7	D6	D5	D4	D3	D2	D1	D0
SME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0	1	0	0	0	0	0	0

5.4.1 High-Pass Filter Bypass

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	HPB	High-Pass Filter Bypass Bit. 0 – AC Coupling High Pass Filter Enabled 1 – AC Coupling High Pass Filter Disabled

The DDXi-2051 features an internal digital high-pass filter for the purpose of DC Blocking. The purpose of this filter is to prevent DC signals from passing through a DDX® amplifier. DC signals can cause speaker damage.

5.4.2 De-Emphasis

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	0	DEMP	De-emphasis: 0 – No De-emphasis 1 – De-emphasis

By setting this bit to HIGH, or one (1), de-emphasis will implemented on all channels. DSPB (DSP Bypass, Bit D2, CFA) bit must be set to 0 for De-emphasis to function.

5.4.3 DSP Bypass

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	DSPB	DSP Bypass Bit: 0 – Normal Operation 1 – Bypass of EQ and Mixing Functionality

Setting the DSPB bit bypasses all the EQ and Mixing functionality of the DDXi-2051 Core.

5.4.4 Post-Scale Link

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	PSL	Post-Scale Link: 0 – Each Channel uses individual Post-Scale value 1 – Each Channel uses Channel 1 Post-Scale value

Post-Scale functionality is an attenuation placed after the volume control and directly before the conversion to PWM. Post-Scale can also be used to limit the maximum modulation index and therefore the peak current. A setting of 1 in the PSL register will result in the use of the value stored in Channel 1 post-scale for all three internal channels.

5.4.5 Biquad Coefficient Link

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	BQL	Biquad Link: 0 – Each Channel uses coefficient values 1 – Each Channel uses Channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the Channel 1 Coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

5.4.6 Dynamic Range Compression/Anti-Clipping Bit

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	DRC	Dynamic Range Compression/Anti-Clipping 0 – Limiters act in Anti-Clipping Mode 1 – Limiters act in Dynamic Range Compression Mode

Both limiters can be used in one of two ways, anti-clipping or dynamic range compression. When used in anti-clipping mode the limiter threshold values are constant and dependent on the limiter settings. In dynamic range compression mode the limiter threshold values vary with the volume settings allowing a nighttime listening mode that provides a reduction in the dynamic range regardless of the volume level.

5.4.7 Zero-Detect Mute Enable

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	1	ZDE	Zero-Detect Mute Enable: Setting of 1 enables the automatic zero-detect mute

Setting the ZDE bit enables the zero-detect automatic mute. When ZDE=1, the zero-detect circuit looks at the input data to each processing channel after the channel-mapping block. If any channel receives 2048 consecutive zero value samples (regardless of fs) then that individual channel is muted (ZDE=1).

5.4.8 Sub-Mix Enable

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	SME	Sub-Mix Enable: 0 – Sub Mix into Left/Right Disabled 1 – Sub Mix into Left/Right Enabled

Setting the SME bit enables a scaled-mix of the content from the Sub channel (i.e. channel 3) into the main Left & Right channels (i.e. channels 1 & 2). The Sub-Mix resides post-volume & gain compression processing.

5.5 Configuration Register E (Address 04h)

D7	D6	D5	D4	D3	D2	D1	D0
SVE	ZCE	*RES*	PWMS	AME	NSBW	MPC	MPCV
1	1	0	0	0	0	1	0

5.5.1 Max Power Correction Variable

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	MPCV	Max Power Correction Variable: 0 – Use Standard MPC Coefficient 1 – Use MPCC bits for MPC Coefficient

By enabling MPC and setting MPCV = 1, the max power correction becomes variable. By adjusting the MPCC registers (address 0x27-0x28) it becomes possible to adjust the THD at maximum unclipped power to a lower value for a particular application.

5.5.2 Max Power Correction

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	1	MPC	Max Power Correction: 0 – MPC Disabled 1 – MPC Enabled

Setting the MPC bit corrects the DDXi-2051 power stage at high power. This mode will lower the THD+N at maximum power output and slightly below.

5.5.3 Noise Shaper BandWidth Selection

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	NSBW	Noise Shaper BandWidth Select 0 – 4th Order Noise Shaper 1 – 3rd Order Noise Shaper

The DDXi-2051 provides the ability to the user to select two types of noise-shaper order. This facilitates the user to essentially make the appropriate bandwidth selection for their design thereby achieving optimal noise performance. **It is recommended to set NSBW = '1' when the device is initialized via I^2C.**

5.5.4 AM Mode Enable

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	AME	AM Mode Enable: 0 – Normal DDX® operation. 1 – AM reduction mode DDX® operation.

The DDXi-2051 features a DDX® processing mode that minimizes the amount of noise generated in the frequency range of AM radio. This mode is intended for use when DDX® is operating in a device with

an active AM tuner. The SNR of the DDX® processing is reduced to ~83dB in this mode, which is still greater than the SNR of AM radio.

5.5.5 PWM Speed Mode

BIT	R/W	RST	NAME	DESCRIPTION
4	R/W	0	PWMS	PWM Speed Selection: Normal or Odd

Table 10 - PWM Output Speed Selections

PWMS (1...0)	PWM Output Speed
0	Normal Speed (384/352.8 kHz for Fs = 48/44.1 kHz) All Channels
1	Odd Speed (341.3/313.6 kHz for Fs = 48/44.1 kHz) All Channels

5.5.6 Zero-Crossing Volume Enable

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	1	ZCE	Zero-Crossing Volume Enable: 1 – Volume adjustments will only occur at digital zero-crossings 0 – Volume adjustments will occur immediately

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings no clicks will be audible.

5.5.7 Soft Volume Update Enable

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	1	SVE	Soft Volume Enable: 1 – Volume adjustments will use soft volume 0 – Volume adjustments will occur immediately

The DDXi-2051 includes a soft volume algorithm that will step through the intermediate volume values at a predetermined rate when a volume change occurs. By setting SVE=0 this can be bypassed and volume changes will jump from old to new value directly. This feature is only available if individual channel volume bypass bit is set to '0'.

5.6 Configuration Register F (Address 05h)

D7	D6	D5	D4	D3	D2	D1	D0
EAPD	PWDN	ECLE	*RES*	BCLE	IDE	OCFG1	OCFG0
0	1	0	1	1	1	0	0

5.6.1 Output Configuration Selection

BIT	R/W	RST	NAME	DESCRIPTION
1…0	R/W	00	OCFG (1…0)	Output Configuration Selection 00 – 2-channel (Full-bridge) Power, 1-channel DDX is default

Table 11 - Output Configuration Selections

OCFG (1...0)	Output Power Configuration
00	2 Channel DDX (Full-Bridge) Power: 1A/1B → 1A/1B 2A/2B → 2A/2B
01	2(Half-Bridge).1(Full-Bridge) Power: 1A → 1A Binary 2A → 1B Binary 3A/3B → 2A/2B Binary
10	*Reserved*
11	1 Channel DDX Mono-Parallel: 3A → 1A/1B 3B → 2A/2B

5.6.2 Invalid Input Detect Mute Enable

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	1	IDE	Invalid Input Detect Auto-Mute Enable: 0 – Disabled 1 – Enabled

Setting the IDE bit enables this function, which looks at the input I^2S data and clocking and will automatically mute all outputs if the signals are perceived as invalid.

5.6.3 Binary Clock Loss Detection Enable

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	1	BCLE	Binary Output Mode Clock Loss Detection Enable 0 – Disabled 1 – Enabled

Detects loss of input MCLK in binary mode and will output 50% duty cycle to prevent audible artifacts when input clocking is lost.

5.6.4 Auto-EAPD on Clock Loss Enable

BIT	R/W	RST	NAME	DESCRIPTION
5	R/W	0	ECLE	Auto EAPD on Clock Loss 0 – Disabled 1 – Enabled

When ECLE is active, it issues a power device power down signal (EAPD) on clock loss detection.

5.6.5 Powerdown

BIT	R/W	RST	NAME	DESCRIPTION
6	R/W	1	PWDN	Software Power Down: 0 – Powerdown mode operation (auto soft-mute enabled) 1 – Normal Operation

If the powerdown bit is set low, a powerdown sequence is initiated resulting in a soft mute of all channels and finally EAPD being asserted approximately .26s later.

5.6.6 External Amplifier Power Down

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	EAPD	External Amplifier Power Down: 0 – External Power Stage Power Down Active 1 – Normal Operation

EAPD is used to actively power down a connected DDX® Power device. This register has to be written to 1 at start-up to enable the DDX® power device for normal operation.

5.7 Volume and Mute Registers

5.7.1 Master Controls

5.7.1.1 Master/Channel Mute Register (Address 06h)

D7	D6	D5	D4	D3	D2	D1	D0
				C3M	C2M	C1M	MMUTE
				0	0	0	0

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	MMute	Master Soft Mute 0 – Normal Operation 1 – Master Soft Mute for All Channels

BIT	R/W	RST	NAME	DESCRIPTION
1	R/W	0	C1M	Channel 1 Mute 0 – Normal Operation 1 – Channel 1 Soft Mute

BIT	R/W	RST	NAME	DESCRIPTION
2	R/W	0	C2M	Channel 2 Soft Mute 0 – Normal Operation 1 – Channel 2 Soft Mute

BIT	R/W	RST	NAME	DESCRIPTION
3	R/W	0	C3M	Channel 3 Soft Mute 0 – Normal Operation 1 – Channel 3 Soft Mute

5.7.1.2 Master Volume Register (Address 07h)

D7	D6	D5	D4	D3	D2	D1	D0
MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
1	1	1	1	1	1	1	1

Note : Value of volume derived from MVOL is dependent on AMV AutoMode Volume settings.

5.7.2 Channel Controls

5.7.2.1 Channel 1 Volume (Address 08h)

D7	D6	D5	D4	D3	D2	D1	D0
C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0	1	1	0	0	0	0	0

5.7.2.2 Channel 2 Volume (Address 09h)

D7	D6	D5	D4	D3	D2	D1	D0
C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0	1	1	0	0	0	0	0

5.7.2.3 Channel 3 Volume (Address 0Ah)

D7	D6	D5	D4	D3	D2	D1	D0
C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0	1	1	0	0	0	0	0

5.7.3 Volume Description

The volume structure of the DDXi-2051 consists of individual volume registers for each of the three channels, a master volume register, and individual channel volume trim registers. The channel volume settings are normally used to set the maximum allowable digital gain and to hard-set gain differences between certain channels. These values are normally set at the initialization of the IC and not changed. The individual channel volumes are adjustable in 0.5dB steps from +48dB to -80 dB. The master volume control is normally mapped to the master volume of the system. The values of these two settings are summed to find the actual gain/volume value for any given channel.

When set to 1, the Master Mute will mute all channels, whereas the individual channel mutes (CxM) will mute only that channel. Both the Master Mute and the Channel Mutes provide a “soft mute” with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate (~96kHz). A “hard mute” can be obtained by commanding a value of all 1’s (FFh) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel whose total volume is less than –100dB will be muted.

All changes in volume take place at zero-crossings when ZCE = 1 (configuration register E) on a per channel basis as this creates the smoothest possible volume transitions. When ZCE=0, volume updates will occur immediately.

The DDXi-2051 also features a soft-volume update function that will ramp the volume between intermediate values when the value is updated, when SVE = 1 (configuration register E). This feature can be disabled by setting SVE = 0.

Each channel also contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel. Also, master soft-mute will not affect the channel if CxVBP = 1.

Each channel also contains a channel mute. If CxM = 1 a soft mute is performed on that channel.

Table 12 - Master Volume Offset as a function of MV (7..0)

MV (7...0)	Volume Offset from Channel Value
00000000 (00h)	0dB
00000001 (01h)	-0.5dB
00000010 (02h)	-1dB
…	…
01001100 (4Ch)	-38dB
…	…
11111110 (FEh)	-127dB
11111111 (FFh)	Hard Master Mute

Table 13 - Channel Volume as a function of CxV (7..0)

CxV (7...0)	Volume
00000000 (00h)	+48dB
00000001 (01h)	+47.5dB
00000010 (02h)	+47dB
…	…
01100001 (5Fh)	+0.5dB
01100000 (60h)	0dB
01011111 (61h)	-0.5dB
…	…
11111110 (FEh)	-79.5 dB
11111111 (FFh)	Hard Channel Mute

5.8 AutoMode Registers

5.8.1 Register – AutoModes EQ, Volume, GC (Address 0Bh)

D7	D6	D5	D4	D3	D2	D1	D0
AMPS		AMGC1	AMGC0	AMV1	AMV0	AMEQ1	AMEQ0
0		0	0	0	0	0	0

Table 14 - AutoMode EQ

AMEQ (1,0)	Mode (Biquad 1-4)
00	User Programmable
01	Preset EQ – PEQ bits
10	Auto Volume Controlled Loudness Curve
11	Not used

By setting AMEQ to any setting other than 00 enables AutoMode EQ. When set, biquads 1-4 are not user programmable. Any coefficient settings for these biquads will be ignored. Also when AutoMode EQ is used the pre-scale value for channels 1-2 becomes hard-set to –18dB.

Table 15 - AutoMode Volume

AMV (1,0)	Mode (MVOL)
00	MVOL 0.5dB 256 Steps (Standard)
01	MVOL Auto Curve 30 Steps
10	MVOL Auto Curve 40 Steps
11	MVOL Auto Curve 50 Steps

Table 16 - AutoMode Gain Compression/Limiters

AMGC (1...0)	Mode
00	User Programmable GC
01	AC No Clipping
10	AC Limited Clipping (10%)
11	DRC Nighttime Listening Mode

AMPS – AutoMode Auto Prescale

BIT	R/W	RST	NAME	DESCRIPTION
7	R/W	0	AMPS	AutoMode Pre-Scale 0 – -18dB used for Pre-scale when AMEQ /= 00 1 – User Defined Pre-scale when AMEQ /= 00

5.8.2 Register – AutoMode AM/Pre-Scale/Bass Management Scale (Address 0Ch)

D7	D6	D5	D4	D3	D2	D1	D0
XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0	0	0	0	0	0	0	0

5.8.2.1 AutoMode AM Switching Enable

BIT	R/W	RST	NAME	DESCRIPTION
0	R/W	0	AMAME	AutoMode AM Enable 0 – Switching Frequency Determined by PWMS Setting 1 – Switching Frequency Determined by AMAM Settings
3…1	R/W	000	AMAM (2…0)	AM Switching Frequency Setting Default: 000

Table 17 - AutoMode AM Switching Frequency Selection

AMAM (2...0)	48kHz/96kHz Input Fs	44.1kHz/88.2kHz Input Fs
000	0.535MHz – 0.720MHz	0.535MHz – 0.670Mhz
001	0.721MHz – 0.900MHz	0.671MHz – 0.800MHz
010	0.901MHz – 1.100MHz	0.801MHz – 1.000MHz
011	1.101MHz – 1.300MHz	1.001MHz – 1.180MHz
100	1.301MHz – 1.480MHz	1.181MHz – 1.340Mhz
101	1.481MHz – 1.600MHz	1.341MHz – 1.500MHz
110	1.601MHz – 1.700MHz	1.501MHz – 1.700MHz

When DDX® is used concurrently with an AM radio tuner, it is advisable to use the AMAM bits to automatically adjust the output PWM switching rate dependent upon the specific radio frequency that the tuner is receiving. The values used in AMAM are also dependent upon the sample rate determined by the ADC used.

5.8.2.2 AutoMode Crossover Setting

BIT	R/W	RST	NAME	DESCRIPTION
7…4	R/W	0	XO (3…0)	AutoMode Crossover Frequency Selection 000 – User Defined Crossover coefficients are used Otherwise – Preset coefficients for the crossover setting desired

The XO bits are used to either select one of the 15 preset crossover frequency settings or enable the user to implement custom crossover filters. The preset crossover settings signify the crossover frequency selected for the 2nd order low pass and 1st order high pass filters used on the processing channels. If a different crossover frequency, other than those available, is desired, then the user needs to set XO = 000 and design custom high-pass and low-pass filters. These filters should then be written to the device coefficient RAM using the I^2C communication. Please refer to section 6.6.

Table 18 - Crossover Frequency Selection

XO (2...0)	Bass Management - Crossover Frequency
0000	User
0001	80 Hz
0010	100 Hz
0011	120 Hz
0100	140 Hz
0101	160 Hz
0110	180 Hz
0111	200 Hz
1000	220 Hz
1001	240 Hz
1010	260 Hz
1011	280 Hz
1100	300 Hz
1101	320 Hz
1110	340 Hz
1111	360 Hz

5.8.3 Register - Preset EQ Settings (Address 0Dh)

D7	D6	D5	D4	D3	D2	D1	D0
			PEQ4	PEQ3	PEQ2	PEQ1	PEQ0
			0	0	0	0	0

Table 19 - Preset EQ Selection

PEQ (3...0)	Setting
00000	Flat
00001	Rock
00010	Soft Rock
00011	Jazz
00100	Classical
00101	Dance
00110	Pop
00111	Soft
01000	Hard
01001	Party
01010	Vocal
01011	Hip-Hop
01100	Dialog
01101	Bass-Boost #1
01110	Bass-Boost #2
01111	Bass-Boost #3
10000	Loudness 1 (least boost)
10001	Loudness 2
10010	Loudness 3
10011	Loudness 4
10100	Loudness 5
10101	Loudness 6
10110	Loudness 7
10111	Loudness 8
11000	Loudness 9
11001	Loudness 10

Table 19 - Preset EQ Selection

PEQ (3...0)	Setting
11010	Loudness 11
11011	Loudness 12
11100	Loudness 13
11101	Loudness 14
11110	Loudness 15 (most boost)

5.9 Channel Configuration Registers

5.9.1 Channel 1 Configuration (Address 0Eh)

D7	D6	D5	D4	D3	D2	D1	D0
C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VBP	C1EQBP	C1TCB
0	0	0	0	0	0	0	0

5.9.2 Channel 2 Configuration (Address 0Fh)

D7	D6	D5	D4	D3	D2	D1	D0
C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VBP	C2EQBP	C2TCB
0	1	0	0	0	0	0	0

5.9.3 Channel 3 Configuration (Address 10h)

D7	D6	D5	D4	D3	D2	D1	D0
C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VBP		
1	0	0	0	0	0		

EQ control can be bypassed on a per channel basis. If EQ control is bypassed on a given channel the prescale and all 9 filters (high-pass, biquads, de-emphasis, bass management cross-over, bass, treble in any combination) are bypassed for that channel.

CxEQBP:

0 – Perform EQ on Channel X – normal operation
1 – Bypass EQ on Channel X

Tone control (bass/treble) can be bypassed on a per channel basis. If tone control is bypassed on a given channel the two filters that tone control utilizes are bypassed.

CxTCB:

0 – Perform Tone Control on Channel x – (default operation)
1 – Bypass Tone Control on Channel x

Each channel can be configured to output either the patented DDX PWM data or standard binary PWM encoded data. By setting the CxBO bit to '1', each channel can be individually controlled to be in binary operation mode.

Also, there is the capability to map each channel independently onto any of the two limiters available within the DDXi-2051 or even not map it to any limiter at all (default mode).

Table 20 - Channel Limiter Mapping Selection

CxLS (1,0)	Channel Limiter Mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2

Each PWM Output Channel can receive data from any channel output of the volume block. Which channel a particular PWM output receives is dependent upon that channel's CxOM register bits.

Table 21 - Channel PWM Output Mapping

CxOM (1...0)	PWM Output From
00	Channel 1
01	Channel 2
10	Channel 3
11	Not used

5.10 Tone Control (Address 11h)

D7	D6	D5	D4	D3	D2	D1	D0
TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0	1	1	1	0	1	1	1

The tone control can provide up to 12dB of boost or cut. When using the tone control, it is recommended to apply a pre-scale of -12dB to guarantee that clipping cannot occur. This can be accomplished by writing a coefficient of 0x200000 to address 0x32 in the coefficient RAM corresponding to the channel 1 pre-scale value. This value should also be written to channel 2 pre-scale.

Table 22 - Tone Control Boost/Cut Selection

BTC (3...0)/TTC (3...0)	Boost/Cut
0000	-12dB
0001	-12dB
…	…
0111	-4dB
0110	-2dB
0111	0dB
1000	+2dB
1001	+4dB
…	…
1101	+12dB
1110	+12dB
1111	+12dB

5.11 Dynamics Control

5.11.1 Limiter 1 Attack/Release Rate (Address 12h)

D7	D6	D5	D4	D3	D2	D1	D0
L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0	1	1	0	1	0	1	0

5.11.2 Limiter 1 Attack/Release Threshold (Address 13h)

D7	D6	D5	D4	D3	D2	D1	D0
L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0	1	1	0	1	0	0	1

5.11.3 Limiter 2 Attack/Release Rate (Address 14h)

D7	D6	D5	D4	D3	D2	D1	D0
L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0	1	1	0	1	0	1	0

5.11.4 Limiter 2 Attack/Release Threshold (Address 15h)

D7	D6	D5	D4	D3	D2	D1	D0
L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0	1	1	0	1	0	0	1

5.11.5 Dynamics Control Description

The DDXi-2051 includes two independent limiter blocks. The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anti-clipping mode, or to actively reduce the dynamic range for a better listening environment (such as a night-time listening mode, which is often needed for DVDs.) The two modes are selected via the DRC bit in Configuration Register D, bit 5 address 0x03. Each channel can be mapped to Limiter1, Limiter2, or not mapped. If a channel is not mapped, that channel will clip normally when 0 dB FS is exceeded. Each limiter will look at the present value of each channel that is mapped to it, select the maximum absolute value of all these channels, perform the limiting algorithm on that value, and then if needed adjust the gain of the mapped channels in unison. The limiter attack thresholds are determined by the LxAT registers. When the Attack Thesehold has been exceeded, the limiter, when active, will automatically start reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. The gain reduction occurs on a peak-detect algorithm.

The release of limiter, when the gain is again increased, is dependent on a RMS-detect algorithm. The output of the volume/limiter block is passed through an RMS filter. The output of this filter is compared to the release threshold, determined by the Release Threshold register. When the RMS filter output falls below the release threshold, the gain is increased at a rate dependent upon the Release Rate register. The gain can never be increased past its set value and therefore the release will only occur if the limiter has already reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range. This is helpful as over-limiting can reduce the dynamic range to virtually zero and cause program material to sound “lifeless”.

In AC mode the attack and release thresholds are set relative to full-scale. In DRC mode the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

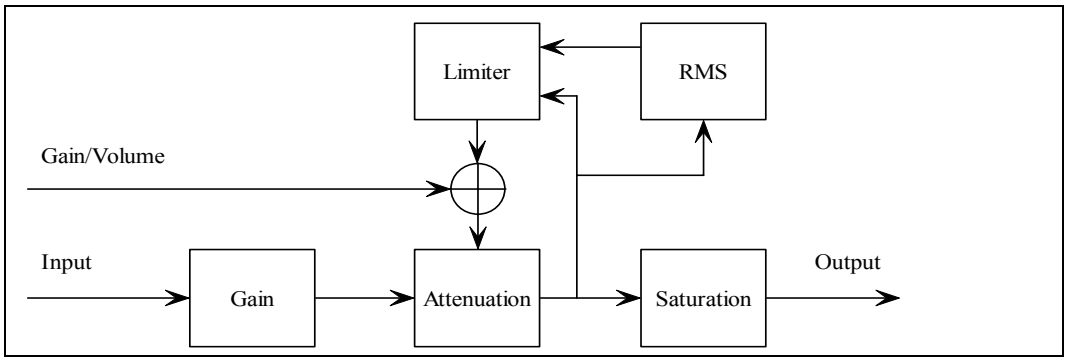


Figure 24 - Basic Limiter and Volume Flow Diagram.

Table 23 - Limiter Attack Rate Selection

LxA (3...0)	Attack Rate dB/ms	
0000	3.1584	Fast
0001	2.7072	
0010	2.2560	
0011	1.8048	
0100	1.3536	
0101	0.9024	
0110	0.4512	
0111	0.2256	
1000	0.1504	
1001	0.1123	
1010	0.0902	
1011	0.0752	
1100	0.0645	
1101	0.0564	
1110	0.0501	
1111	0.0451	Slow

Table 24 - Limiter Release Rate Selection

LxR (3...0)	Release Rate dB/ms	
0000	0.5116	Fast
0001	0.1370	
0010	0.0744	
0011	0.0499	
0100	0.0360	
0101	0.0299	
0110	0.0264	
0111	0.0208	
1000	0.0198	
1001	0.0172	
1010	0.0147	
1011	0.0137	
1100	0.0134	
1101	0.0117	
1110	0.0110	
1111	0.0104	Slow

Anti-Clipping Mode

Table 25 - Limiter Attack Threshold Selection (AC-Mode).

LxAT (3...0)	AC (dB relative to FS)
0000	-12
0001	-10
0010	-8
0011	-6
0100	-4
0101	-2
0110	0
0111	+2
1000	+3
1001	+4
1010	+5
1011	+6
1100	+7
1101	+8
1110	+9
1111	+10

Table 26 - Limiter Release Threshold Selection (AC-Mode).

LxRT (3...0)	AC (dB relative to FS)
0000	-∞
0001	-29dB
0010	-20dB
0011	-16dB
0100	-14dB
0101	-12dB
0110	-10dB
0111	-8dB
1000	-7dB
1001	-6dB
1010	-5dB
1011	-4dB
1100	-3dB
1101	-2dB
1110	-1dB
1111	-0dB

Dynamic Range Compression Mode

Table 27 - Limiter Attack Threshold Selection (DRC-Mode).

LxAT (3...0)	DRC (dB relative to Volume)
0000	-31
0001	-29
0010	-27
0011	-25
0100	-23
0101	-21

Table 28 - Limiter Release Threshold Selection (DRC-Mode).

LxRT (3...0)	DRC (db relative to Volume + LxAT)
0000	-∞
0001	-38dB
0010	-36dB
0011	-33dB
0100	-31dB
0101	-30dB

Table 27 - Limiter Attack Threshold Selection (DRC-Mode).

LxAT (3...0)	DRC (dB relative to Volume)
0110	-19
0111	-17
1000	-16
1001	-15
1010	-14
1011	-13
1100	-12
1101	-10
1110	-7
1111	-4

Table 28 - Limiter Release Threshold Selection (DRC-Mode).

LxRT (3...0)	DRC (db relative to Volume + LxAT)
0110	-28dB
0111	-26dB
1000	-24dB
1001	-22dB
1010	-20dB
1011	-18dB
1100	-15dB
1101	-12dB
1110	-9dB
1111	-6dB

6.0 USER PROGRAMMABLE PROCESSING

6.1 EQ – Biquad Equation

The biquads use the equation that follows. This is diagrammed in Figure 25 below.

$$Y[n] = 2(b_0/2)X[n] + 2(b_1/2)X[n-1] + b_2X[n-2] – 2(a_1/2)Y[n-1] – a_2Y[n-2]$$

$$= b_0X[n] + b_1X[n-1] + b_2X[n-2] – a_1Y[n-1] – a_2Y[n-2]$$

where Y[n] represents the output and X[n] represents the input. Multipliers are 24-bit signed fractional multipliers, with coefficient values in the range of 800000h (-1) to 7FFFFFh (0.9999998808).

Coefficients stored in the User Defined Coefficient RAM are referenced in the following manner:

CxHy0 = $b_1/2$

CxHy1 = b_2

CxHy2 = $-a_1/2$

CxHy3 = $-a_2$

CxHy4 = $b_0/2$

The x represents the channel and the y the biquad number. For example C3H41 is the $b_0/2$ coefficient in the fourth biquad for channel 3

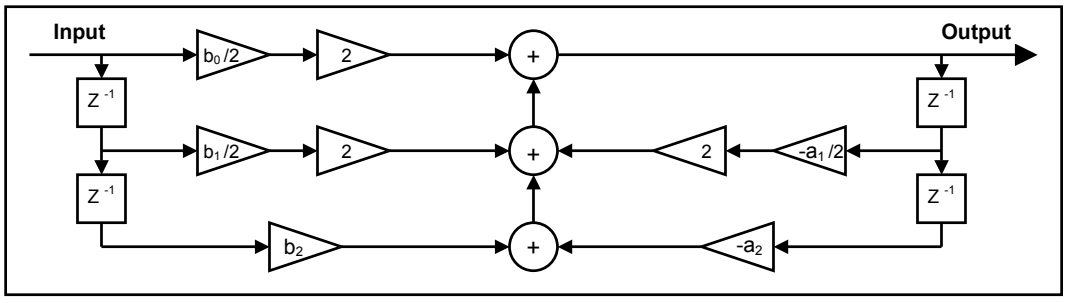


Figure 25 - Biquad Filter Structure

6.2 Pre-Scale

The Pre-Scale block which precedes the first biquad is used for attenuation when filters are designed that boost frequencies above 0dBFS. This is a single 24-bit signed multiplier, with 800000h = -1 and 7FFFFFh = 0.9999998808. By default, all pre-scale factors are set to 7FFFFFh.

6.3 Post-Scale

The DDXi-2051 provides one additional multiplication after the last interpolation stage and before the distortion compensation on each channel. This is a 24-bit signed fractional multiplier. The scale factor for this multiplier is loaded into RAM using the same I^2C registers as the biquad coefficients and the mix. All channels can use the same settings as channel 1 by setting the post-scale link bit.

6.4 Mix/Bass Management

The DDXi-2051 provides a post-EQ mixing block for each channel. Each channel has two mixing coefficients, which are 24-bit signed fractional multipliers, that correspond to the two channels of input to the mixing block. These coefficients are accessible via the User Controlled Coefficient RAM described below. The mix coefficients are expressed as 24-bit signed; fractional numbers in the range +1.0 (8388607) to –1.0 (-8388608) are used used to provide three channels of output from two channels of filtered input.

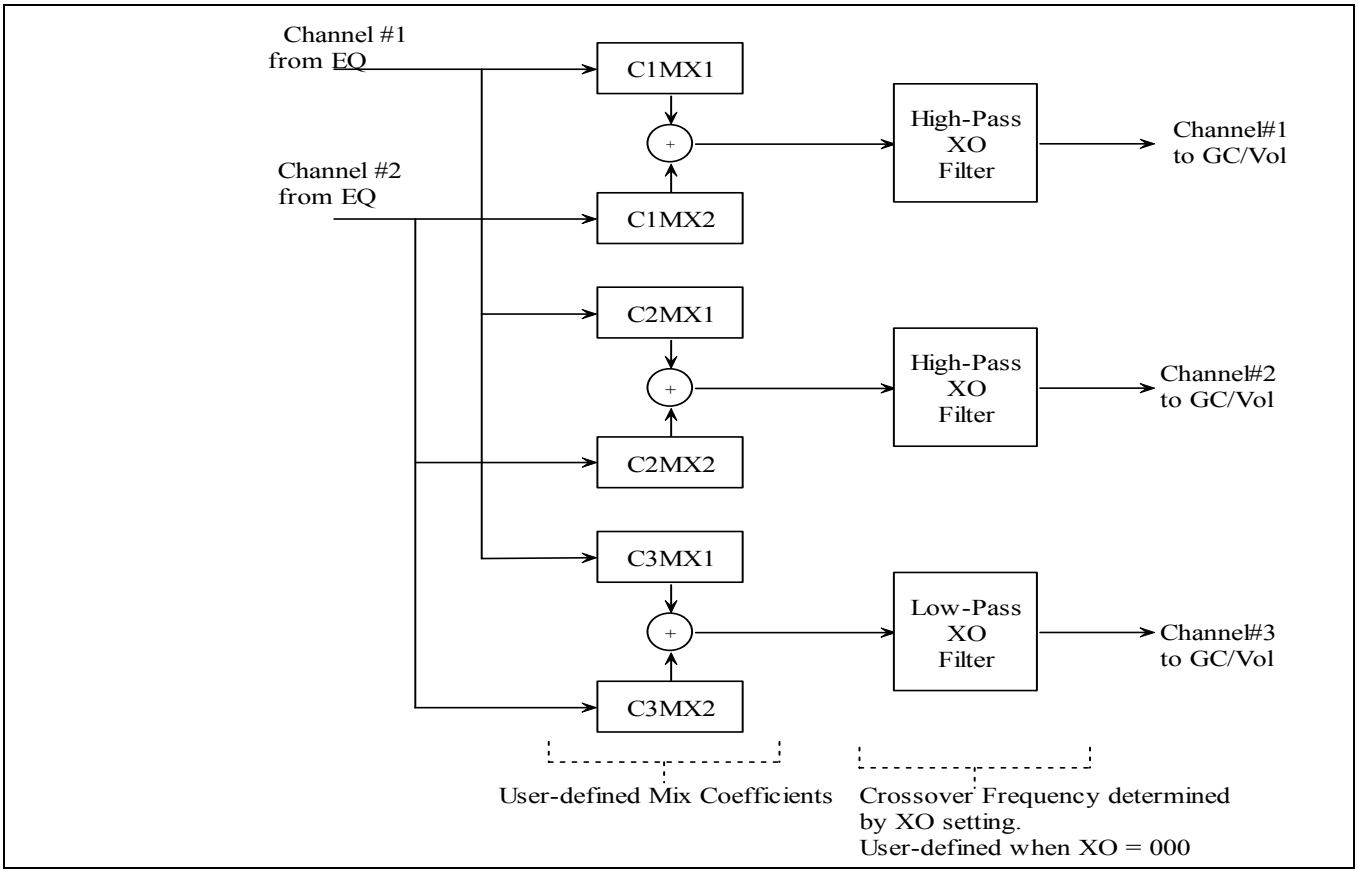


Figure 26 - Mix/Bass Management Block Diagram

After a mix is achieved, the DDXi-2051 also provides the capability to implement crossver filters on all channels corresponding to 2.1 bass management solution. Channels 1-2 use a 1st order high-pass filter and channel 3 uses a 2nd order low-pass filter corresponding to the setting of the XO bits of I2C register 0Ch. If XO = 000, user specified crossover filters are used. By default these coefficients correspond to pass-through. However, the user can write these coefficients in a similar way as the EQ biquads. When user-defined setting is selected, the user can only write 2nd order crossover filters. This output is then passed on to the Volume/Limiter block.

6.5 Calculating 24-Bit Signed Fractional Numbers from a dB Value

The pre-scale, mixing, and post-scale functions of the DDXi-2051 use 24-bit signed fractional multipliers to attenuate signals. These attenuations can also invert the phase and therefore range in value from –1 to +1. It is possible to calculate the coefficient to utilize for a given negative dB value (attenuation) via the equations below.

Non-Inverting Phase Numbers 0 to +1 :

Coefficient = Round(8388607 * 10^(dB/20))

Inverting Phase Numbers 0 to –1 :

Coefficient = 16777216 - Round(8388607 * 10^(dB/20))

As can be seen by the preceding equations, the value for positive phase 0dB is 0x7FFFFF and the value for negative phase 0dB is 0x800000.

6.6 User Defined Coefficient RAM

6.6.1 Coefficient Address Register 1 (Address 16h)

D7	D6	D5	D4	D3	D2	D1	D0
CFA7	CFA6	CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0	0	0	0	0	0	0	0

6.6.2 Coefficient b1Data Register Bits 23...16 (Address 17h)

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

6.6.3 Coefficient b1Data Register Bits 15...8 (Address 18h)

D7	D6	D5	D4	D3	D2	D1	D0
C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0	0	0	0	0	0	0	0

6.6.4 Coefficient b1Data Register Bits 7...0 (Address 19h)

D7	D6	D5	D4	D3	D2	D1	D0
C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0	0	0	0	0	0	0	0

6.6.5 Coefficient b2 Data Register Bits 23...16 (Address 1Ah)

D7	D6	D5	D4	D3	D2	D1	D0
C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0	0	0	0	0	0	0	0

6.6.6 Coefficient b2 Data Register Bits 15...8 (Address 1Bh)

D7	D6	D5	D4	D3	D2	D1	D0
C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0	0	0	0	0	0	0	0

6.6.7 Coefficient b2 Data Register Bits 7...0 (Address 1Ch)

D7	D6	D5	D4	D3	D2	D1	D0
C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0	0	0	0	0	0	0	0

6.6.8 Coefficient a1 Data Register Bits 23...16 (Address 1Dh)

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

6.6.9 Coefficient a1 Data Register Bits 15...8 (Address 1Eh)

D7	D6	D5	D4	D3	D2	D1	D0
C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0	0	0	0	0	0	0	0

6.6.10 Coefficient a1 Data Register Bits 7...0 (Address 1Fh)

D7	D6	D5	D4	D3	D2	D1	D0
C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0	0	0	0	0	0	0	0

6.6.11 Coefficient a2 Data Register Bits 23...16 (Address 20h)

D7	D6	D5	D4	D3	D2	D1	D0
C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0	0	0	0	0	0	0	0

6.6.12 Coefficient a2 Data Register Bits 15...8 (Address 21h)

D7	D6	D5	D4	D3	D2	D1	D0
C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0	0	0	0	0	0	0	0

6.6.13 Coefficient a2 Data Register Bits 7...0 (Address 22h)

D7	D6	D5	D4	D3	D2	D1	D0
C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0	0	0	0	0	0	0	0

6.6.14 Coefficient b0 Data Register Bits 23...16 (Address 23h)

D7	D6	D5	D4	D3	D2	D1	D0
C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0	0	0	0	0	0	0	0

6.6.15 Coefficient b0 Data Register Bits 15...8 (Address 24h)

D7	D6	D5	D4	D3	D2	D1	D0
C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0	0	0	0	0	0	0	0

6.6.16 Coefficient b0 Data Register Bits 7...0 (Address 25h)

D7	D6	D5	D4	D3	D2	D1	D0
C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0	0	0	0	0	0	0	0

6.6.17 Coefficient Write Control Register (Address 26h)

D7	D6	D5	D4	D3	D2	D1	D0
				RA	R1	WA	W1
				0	0	0	0

Coefficients for EQ, Mix, and Scaling are handled internally in the DDXi-2051 via RAM. Access to this RAM is available to the user via an I^2C register interface. A collection of I^2C registers are dedicated to this function. First register contains the coefficient base address, five sets of three registers store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the read or write of the coefficient (s) to RAM. The following are instructions for reading and writing coefficients.

Reading a coefficient from RAM

- Write 8-bits of address to I^2C register 16h
- Write '1' to bit R1 (D2) of I^2C register 26h
- Read top 8-bits of coefficient in I^2C address 17h
- Read middle 8-bits of coefficient in I^2C address 18h
- Read bottom 8-bits of coefficient in I^2C address 19h

Reading a set of coefficients from RAM

- Write 8-bits of address to I^2C register 16h
- Write '1' to bit RA (D3) of I^2C register 26h
- Read top 8-bits of coefficient in I^2C address 17h
- Read middle 8-bits of coefficient in I^2C address 18h
- Read bottom 8-bits of coefficient in I^2C address 19h
- Read top 8-bits of coefficient b2 in I^2C address 1Ah
- Read middle 8-bits of coefficient b2 in I^2C address 1Bh
- Read bottom 8-bits of coefficient b2 in I^2C address 1Ch

- Read top 8-bits of coefficient a1 in I²C address 1Dh
- Read middle 8-bits of coefficient a1 in I²C address 1Eh
- Read bottom 8-bits of coefficient a1 in I²C address 1Fh
- Read top 8-bits of coefficient a2 in I²C address 20h
- Read middle 8-bits of coefficient a2 in I²C address 21h
- Read bottom 8-bits of coefficient a2 in I²C address 22h
- Read top 8-bits of coefficient b0 in I²C address 23h
- Read middle 8-bits of coefficient b0 in I²C address 24h
- Read bottom 8-bits of coefficient b0 in I²C address 25h

Writing a single coefficient to RAM

- Write 8-bits of address to I²C register 16h
- Write top 8-bits of coefficient in I²C address 17h
- Write middle 8-bits of coefficient in I²C address 18h
- Write bottom 8-bits of coefficient in I²C address 19h
- Write 1 to W1 bit in I²C address 26h

Writing a set of coefficients to RAM

- Write 8-bits of starting address to I²C register 16h
- Write top 8-bits of coefficient b1 in I²C address 17h
- Write middle 8-bits of coefficient b1 in I²C address 18h
- Write bottom 8-bits of coefficient b1 in I²C address 19h
- Write top 8-bits of coefficient b2 in I²C address 1Ah
- Write middle 8-bits of coefficient b2 in I²C address 1Bh
- Write bottom 8-bits of coefficient b2 in I²C address 1Ch
- Write top 8-bits of coefficient a1 in I²C address 1Dh
- Write middle 8-bits of coefficient a1 in I²C address 1Eh
- Write bottom 8-bits of coefficient a1 in I²C address 1Fh
- Write top 8-bits of coefficient a2 in I²C address 20h
- Write middle 8-bits of coefficient a2 in I²C address 21h
- Write bottom 8-bits of coefficient a2 in I²C address 22h
- Write top 8-bits of coefficient b0 in I²C address 23h
- Write middle 8-bits of coefficient b0 in I²C address 24h
- Write bottom 8-bits of coefficient b0 in I²C address 25h
- Write 1 to WA bit in I²C address 26h

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side-effects. When using this technique, the 8-bit address would specify the address of the biquad b1 coefficient (e.g. 0, 5, 10, 15, …, 45 decimal), and the DDXi-2051 will generate the RAM addresses as offsets from this base value to write the complete set of coefficient data.

Table 29 - RAM Block for Biquads, Mixing, and Scaling

Index (Decimal)	Index (Hex)		Coefficient	Default
0	00h	Channel 1 – Biquad 1	C1H10 (b1/2)	000000h
1	01h		C1H11 (b2)	000000h
2	02h		C1H12 (a1/2)	000000h
3	03h		C1H13 (a2)	000000h
4	04h		C1H14 (b0/2)	400000h
5	05h	Channel 1 – Biquad 2	C1H20	000000h
…	…	…	…	…
19	13h	Channel 1 – Biquad 4	C1H44	400000h
20	14h	Channel 2 – Biquad 1	C2H10	000000h
21	15h		C2H11	000000h
…	…	…	…	…
39	27h	Channel 2 – Biquad 4	C2H44	400000h
40	28h	High-Pass 2nd Order Filter For XO = 000	C12H0 (b1/2)	000000h
41	29h		C12H1 (b2)	000000h
42	2Ah		C12H2 (a1/2)	000000h
43	2Bh		C12H3 (a2)	000000h
44	2Ch		C12H4 (b0/2)	400000h
45	2Dh	Low-Pass 2nd Order Filter For XO = 000	C12L0 (b1/2)	000000h
46	2Eh		C12L1 (b2)	000000h
47	2Fh		C12L2 (a1/2)	000000h
48	30h		C12L3 (a2)	000000h
49	31h		C12L4 (b0/2)	400000h
50	32h	Channel 1 – Pre-Scale	C1PreS	7FFFFFh
51	33h	Channel 2 – Pre-Scale	C2PreS	7FFFFFh
52	34h	Channel 1 – Post-Scale	C1PstS	7FFFFFh
53	35h	Channel 2 – Post-Scale	C2PstS	7FFFFFh
54	36h	Channel 3 – Post-Scale	C3PstS	7FFFFFh
55	37h	Thermal Warning – Post Scale	TWPstS	5A9DF7h
56	38h	Channel 1 – Mix 1	C1MX1	7FFFFFh
57	39h	Channel 1 – Mix 2	C1MX2	000000h
58	3Ah	Channel 2 – Mix 1	C2MX1	000000h
59	3Bh	Channel 2 – Mix 2	C2MX2	7FFFFFh
60	3Ch	Channel 3 – Mix 1	C3MX1	400000h
61	3Dh	Channel 3 – Mix 2	C3MX2	400000h
62	3Eh	UNUSED		
63	3Fh	UNUSED		

6.7 Variable MAX Power Correction (Address 27h-28h):

MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1.

D7	D6	D5	D4	D3	D2	D1	D0
MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0	0	1	0	1	1	0	1
MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
1	1	0	0	0	0	0	0

6.8 Fault Detect Recovery (Address 2Bh-2Ch):

FDRC bits specify the 16-bit Fault Detect Recovery time delay. When FAULT is asserted, the TRISTATE output will be immediately asserted low and held low for the time period specified by this constant. A constant value of 0001h in this register is ~.083ms. The default value of 000C specifies ~.1mSec.

D7	D6	D5	D4	D3	D2	D1	D0
FRDC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0	0	0	0	1	1	0	0

6.9 Status Indicator Register (Address 2Dh)

D7	D6	D5	D4	D3	D2	D1	D0
PLLUL						FAULT	TWARN
0						1	1

Status Register bits serve the purpose of communicating the detected error or warning condition to the user. This is a read-only register and writing to this register would not be of any consequence.

6.9.1 Thermal Warning Indicator

BIT	R/W	RST	NAME	DESCRIPTION
0	R	1	TWARN	Thermal Warning Indicator 0 – Thermal Warning detected 1 – Normal Operation (No Thermal Warning)

If the power stage thermal operating conditions are exceeded, it transmits a thermal warning to the digital logic block to initiate a corrective procedure. This register bit is set to '0' to indicate its occurrence and it reverts back to its default state as soon as the cause of the thermal warning has been corrected.

6.9.2 Fault Detect Indicator

BIT	R/W	RST	NAME	DESCRIPTION
1	R	1	FAULT	Fault Indicator 0 – Fault issued from the power stage 1 – Normal Operation (No Fault)

As soon as the power stage issues a Fault error signal, thereby initiating the Fault recovery procedure described in Section 6.8, this register bit is set to '0' to indicate to the user of such a condition. As soon as the fault condition (over-current or thermal) is corrected, this bit is reset back to its default state.

6.9.3 PLL Unlock Indicator

BIT	R/W	RST	NAME	DESCRIPTION
7	R	0	PLLUL	PLL Unlock Indicator 0 – Normal Operation (PLL is in a locked state) 1 – PLL Unlock is detected (due to probable clock loss)

The PLL, operating under normal conditions needs an adequate clock, is locked into an internal oscillating frequency. However, if the clock is insufficient or if it is abruptly lost, the PLL lock state is lost and this information is relayed to the user via setting the PLLUL bit of the Status register to '1'. As soon as the PLL reverts back to a locked state, this bit is set to '0'.

7.0 DESIGN INFORMATION

7.1 Output Power vs. Supply Voltage

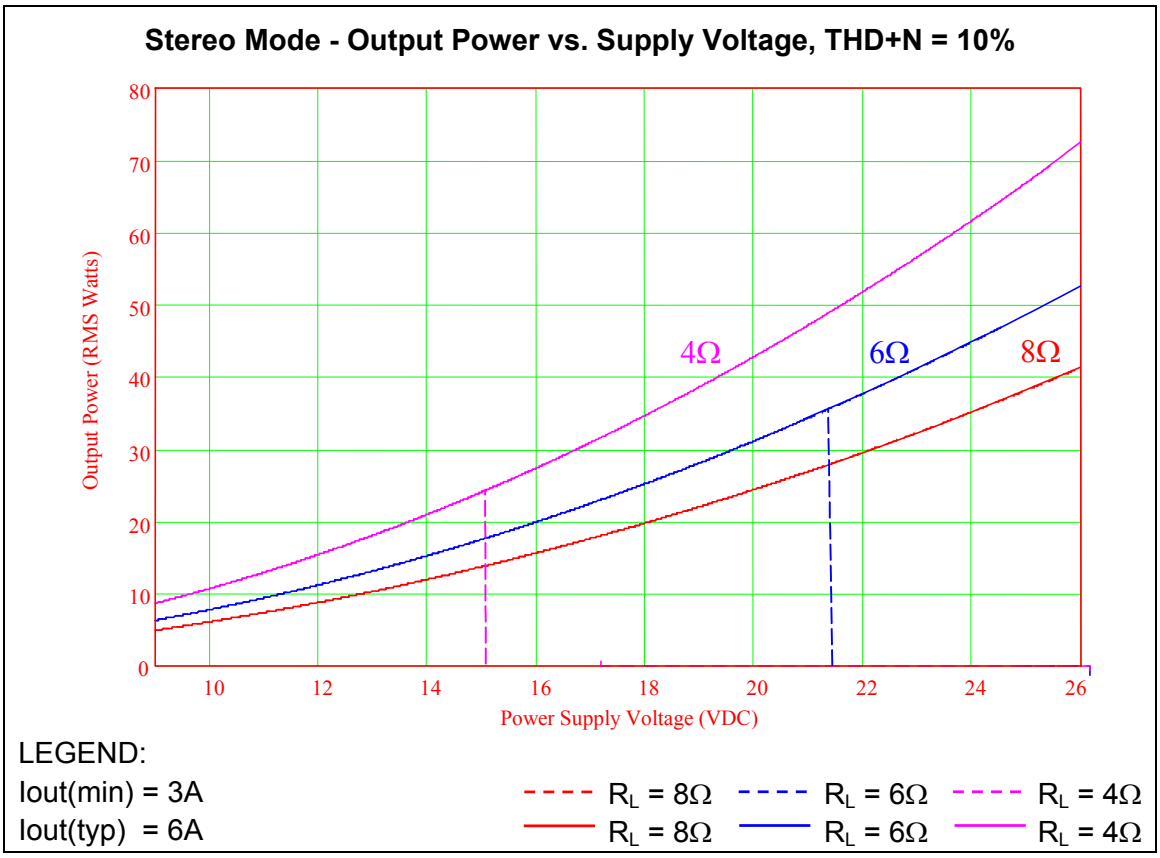


Figure 27 - Output Power vs. Supply Voltage for Stereo Bridge [Note 7]

Note 7 - Output power at <1% THD is approximately 22% lower

Figure 27 shows the full-scale output power (0dB FS digital input with unity amplifier gain) as a function of Power Supply Voltage for 4, 6, and 8 Ohm loads in either DDX® Mode or Binary Full Bridge Mode. Output power is constrained for higher impedance loads by the maximum voltage limit of the DDXi-2051 IC and by the over-current protection limit for lower impedance loads. The minimum threshold for the over-current protection circuit of the DDXi-2051 is 3A (at 25 ºC) but the typical threshold is 6A for the device. The solid curves depict typical output power capability of the device. The dotted curves depicts the output power capability constrained to the minimum current specification of the DDXi-2051. The output power curves assume proper thermal management of the power device's internal dissipation.

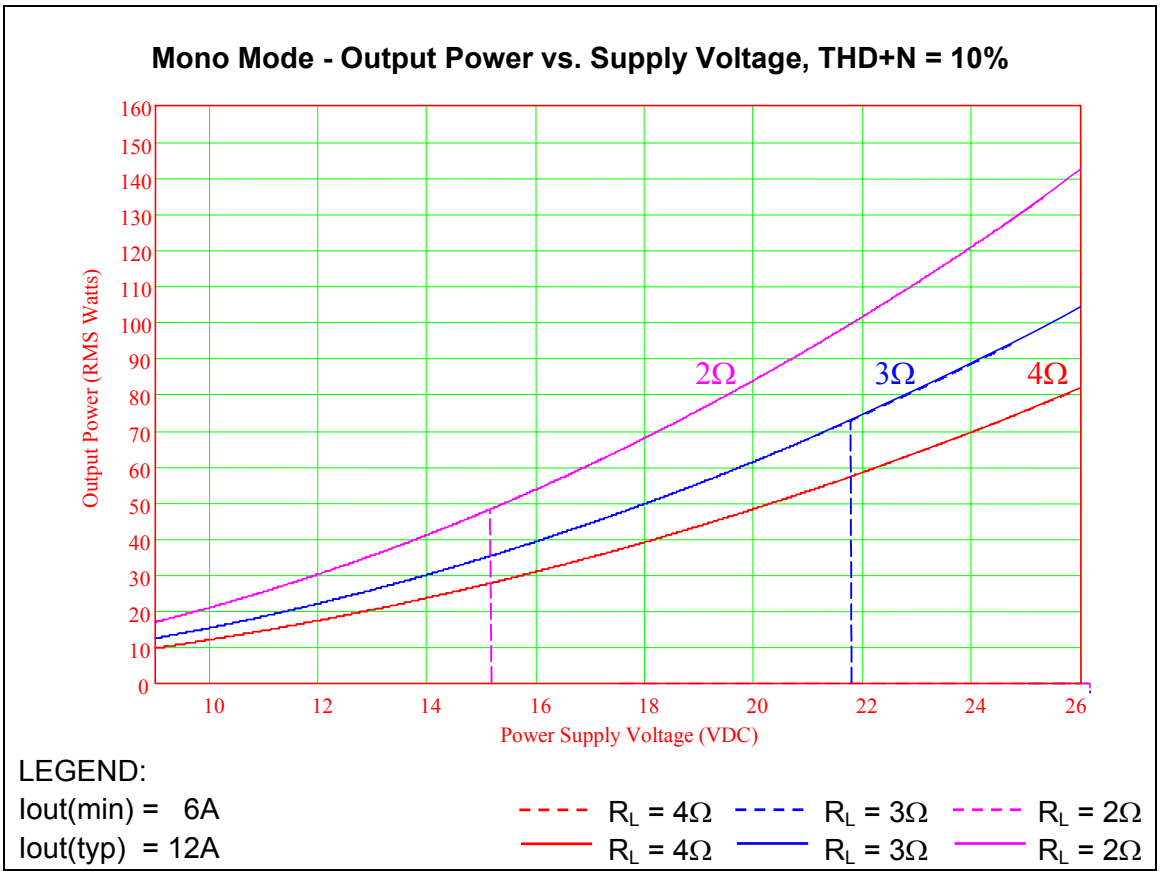


Figure 28 - Mono Bridge Output, DDX Mode Only, Power vs. Supply [Note 8]

Note 8 - Output power at <1% THD is approximately 22% lower

Figure 28 depicts the mono mode output power as a function of power supply voltages for loads of 2, 3, and 4 Ohms. The same current limit observations from Figure 27 apply, except output current for the DDXi-2051 is 6A minimum, with 12A typical in mono bridge configuration. The solid curves depict typical performance and dashed curves depict the minimum current limit. Again, the output power curves assume proper thermal management of the power device's internal dissipation.

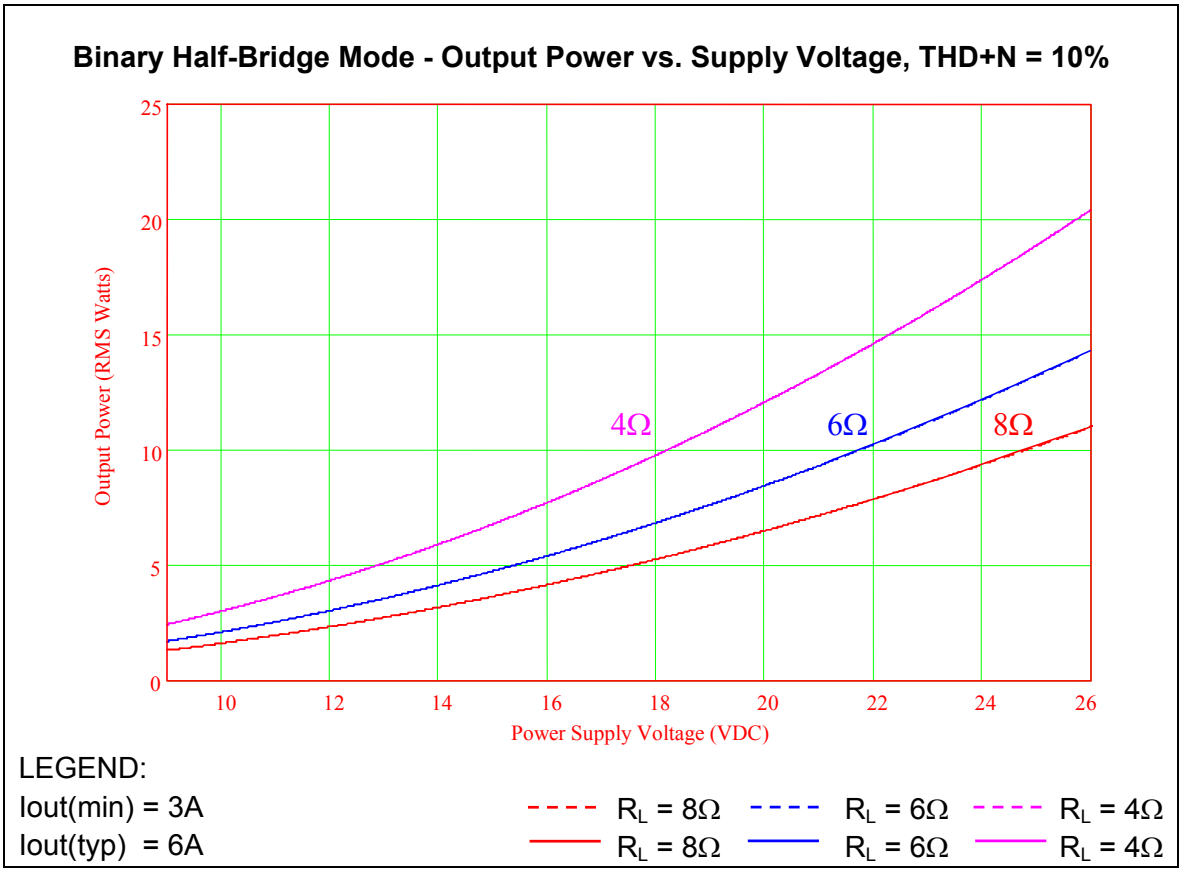


Figure 29 - Half-Bridge Binary Mode Output Power vs Supply [Note 9] [Note 10]

Note 9 - Output power at <1% THD is approximately 22% lower.

Note 10 - Curves taken at f = 1 kHz and using a 330uF blocking capacitor.

Figure 29 depicts the output power as a function of power supply voltages for loads of 4, 6, and 8 Ohms when the DDXi-2051 is operated in a half-bridge Binary Mode. The solid curves depict typical performance. Minimum current limit is not reached for these combinations of voltage and load impedance. Once again, the output power curves assume proper thermal management of the power device's internal dissipation.

7.2 Power Supply and Control Sequencing.

Figure 30 shows the recommended power-up and power-down sequencing. The “time zero” reference point is taken where Vcc crosses the Undervoltage Lockout threshold.

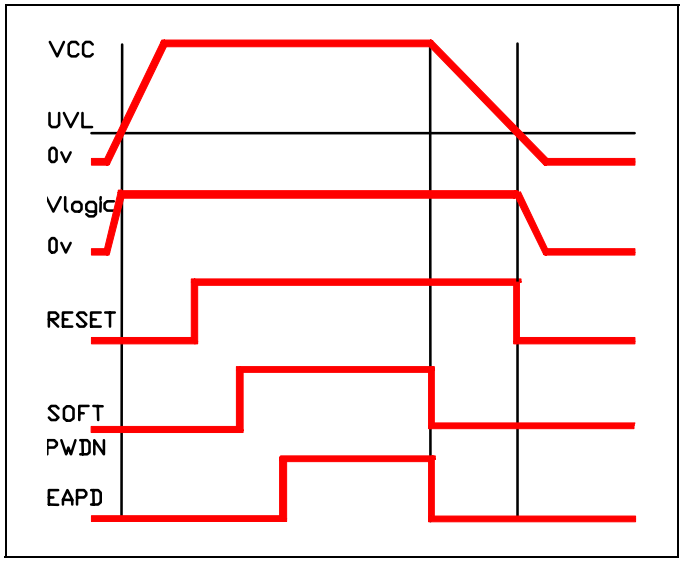


Figure 30 – Recommended Power-Up & Power-Down Sequence

7.3 Schematic Diagrams

Table 30 - Component Selection "Table A" - Full-Bridge Operation

Load	Inductor	Capacitor
4Ω	10uH	1.0uF
6Ω	15uH	470nF
8Ω	22uH	470nF

Table 31 - Component Selection "Table B" - Binary Half-Bridge Operation

Load	Inductor	Capacitor
4Ω	22uH	680nF
6Ω	33uH	470nF
8Ω	47uH	390nF

Table 32 - Component Selection "Table C" - Mono Operation

Load	Inductor	Capacitor
2Ω	4.7uH	2.0uF
3Ω	6.8uH	1.0uF
4Ω	10uH	1.0uF

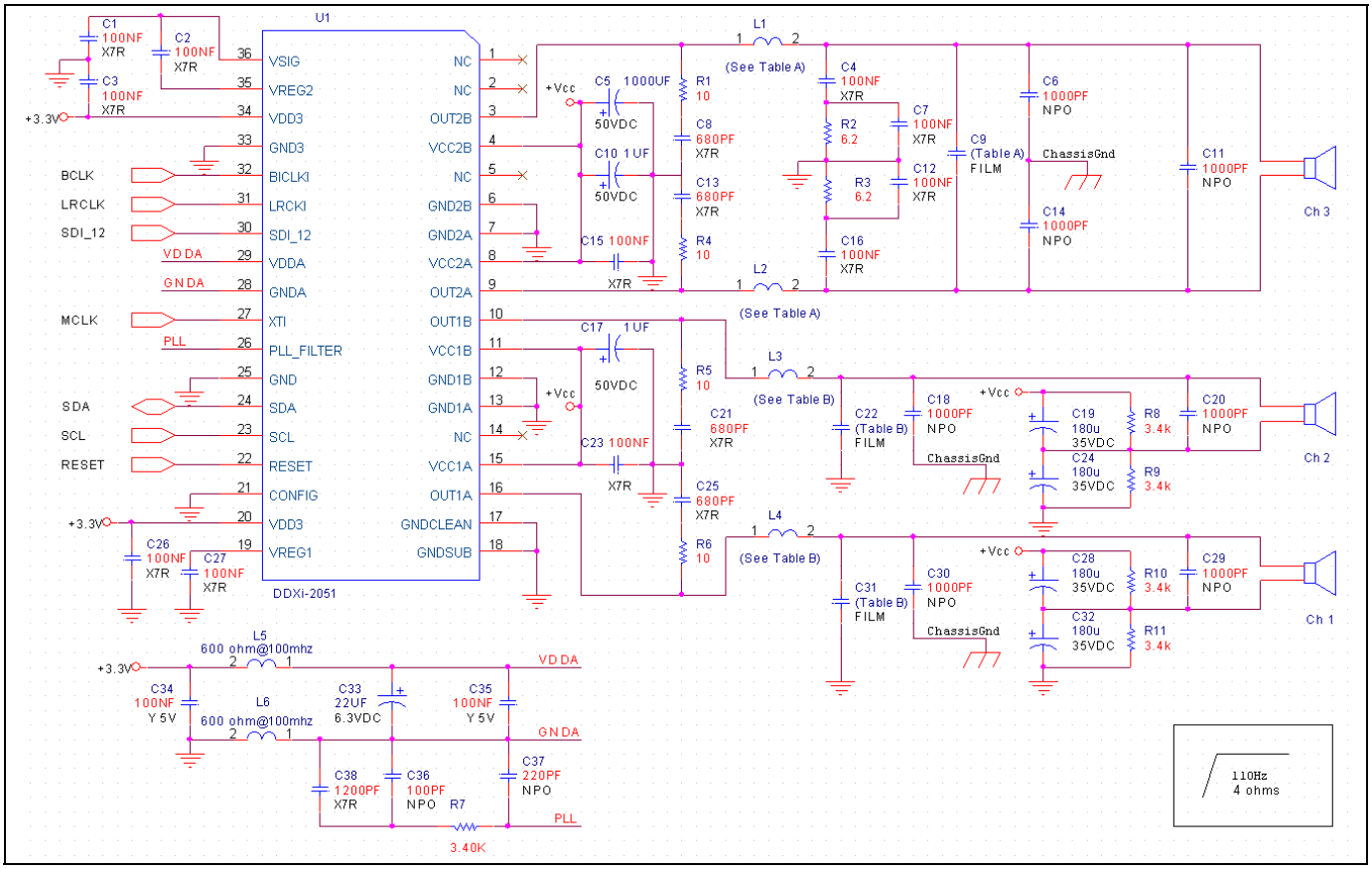


Figure 31 - Schematic Diagram for 2 (Half-bridge) channels + 1 (Full-bridge)-channel On-board Power.

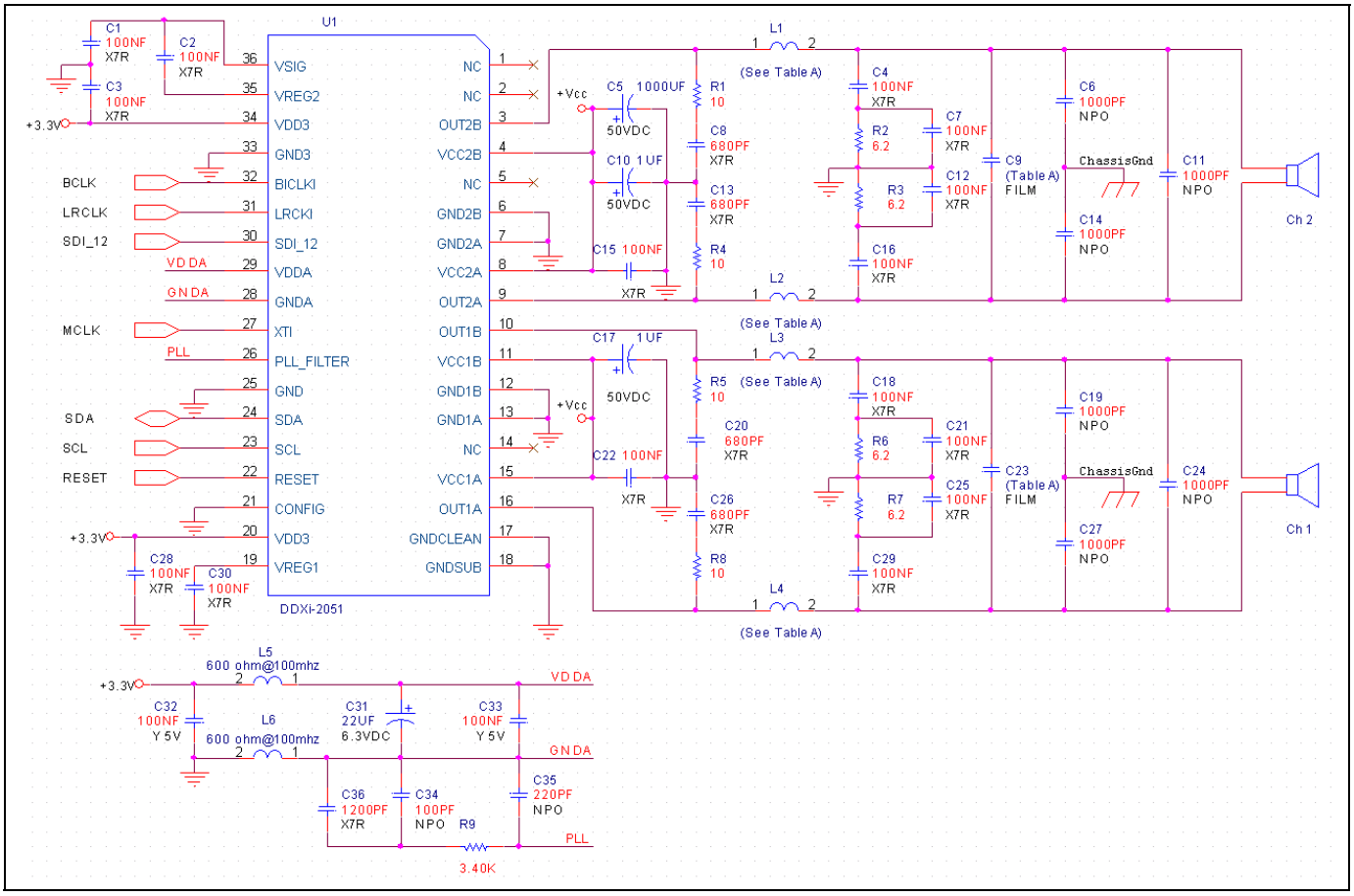


Figure 32 - Schematic Diagram for 2-channel (Full-bridge) Power.

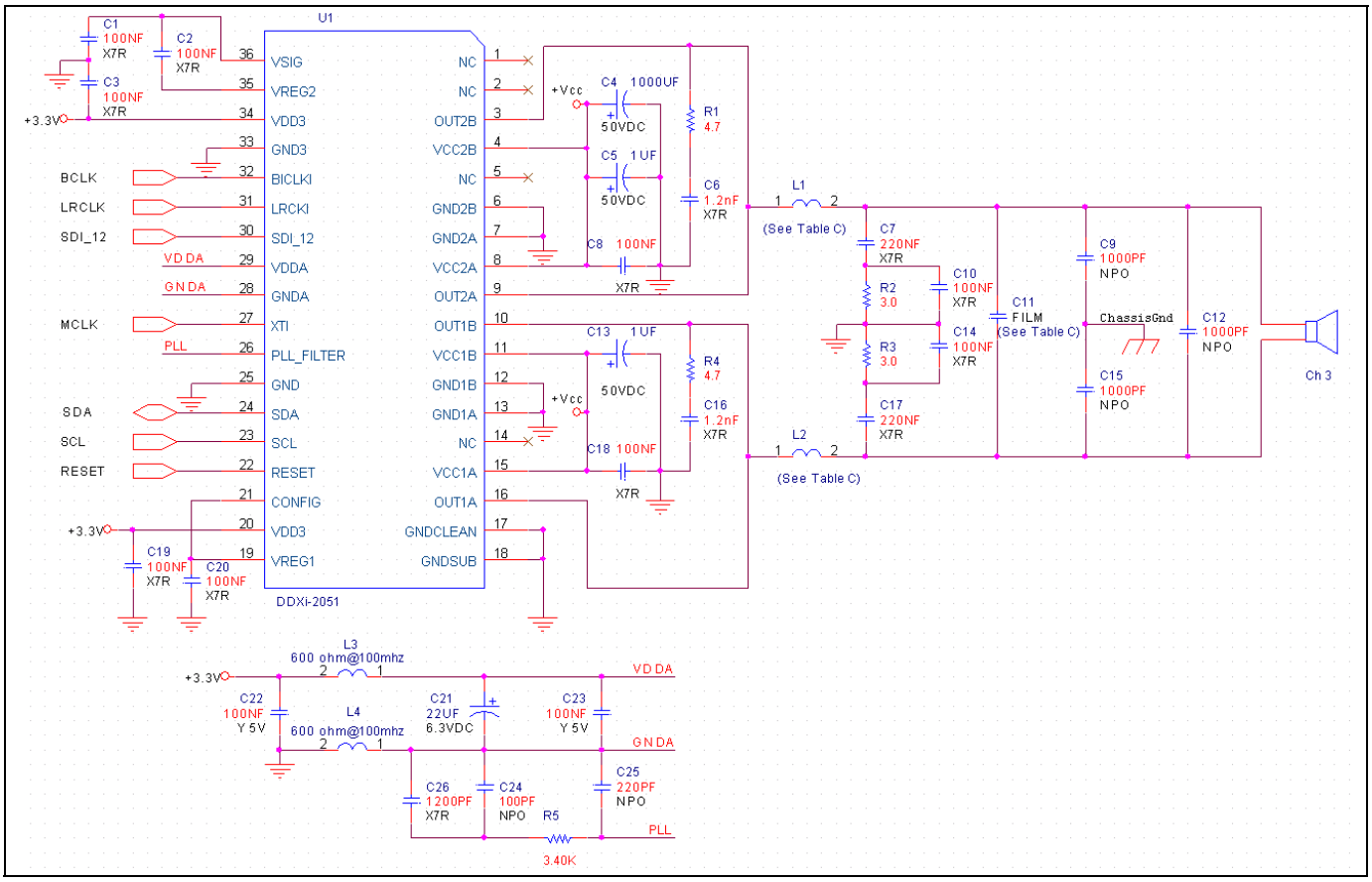


Figure 33 - Schematic Diagram for 1-channel Mono-Parallel Power.

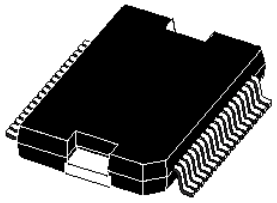
8.0 PACKAGE INFORMATION

8.1 Package Outline Drawing

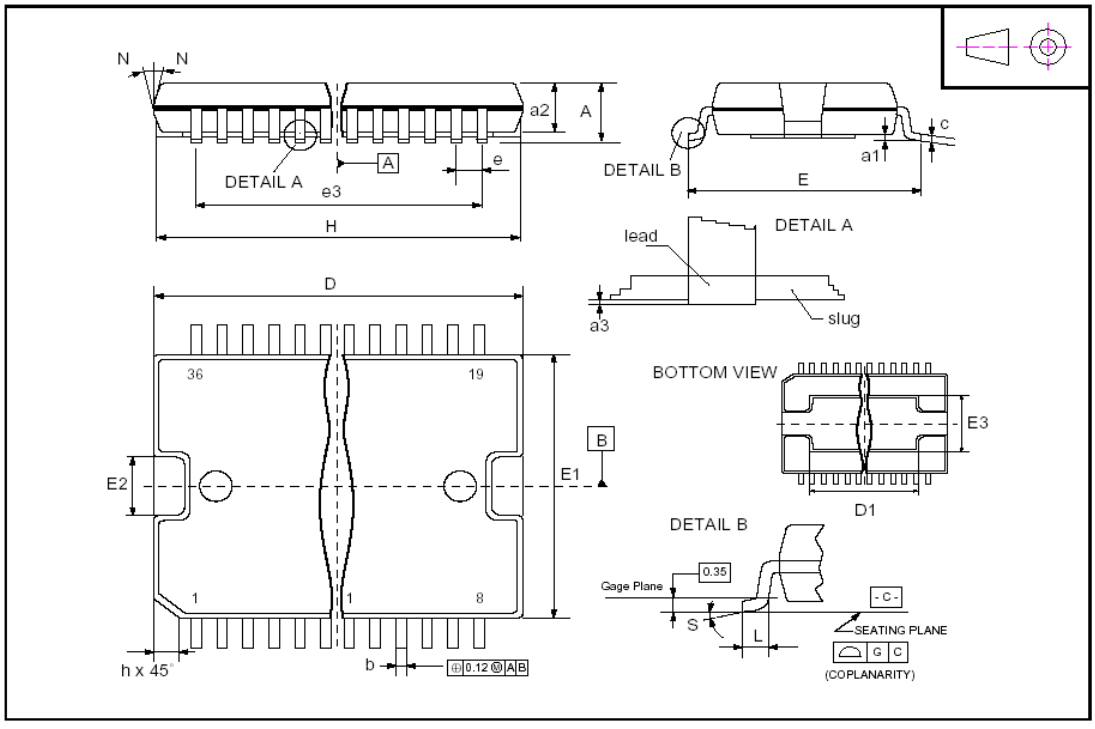
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.141
a1	0.10		0.30	0.004		0.012
a2			3.30			0.130
a3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D (1)	15.80		16.00	0.622		0.630
D1	9.40		9.80	0.370		0.385
E	13.90		14.50	0.547		0.570
e		0.65			0.0256	
e3		11.05			0.435	
E1 (1)	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
E4	2.90		3.20	0.114		0.126
G	0		0.10	0		0.004
H	15.50		15.90	0.610		0.626
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	8 °(max.)					

(1): "D" and "E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA

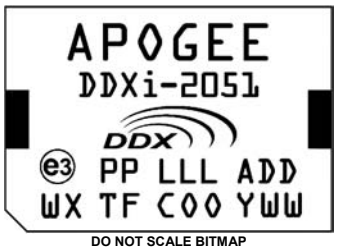


PowerSO-36 Multichip



Specifications are subject to change without notice.

8.2 Marking Configuration



DO NOT SCALE BITMAP

LEGEND:

PPLLLADDWXTF	Traceability Coding
COO	Country Of Origin
Y	Assembly Year
WW	Assembly Week
e3	Pb-Free (RoHS Compliant) (no symbol if not Pb-Free)