All-Digital High Efficiency Power Amplifiers

FEATURES

- HIGH OUTPUT CAPABILITY
- **DDX® Mono-Mode:**
  - **DDX-2062:** 1 x 90 W, 4Ω, <10% THD
  - **DDX-2052:** 1 x 80 W, 4Ω, <10% THD
- **DDX® Full-Bridge Mode:**
  - **DDX-2062:** 2 x 45 W, 8Ω, <10% THD
  - **DDX-2052:** 2 x 40 W, 8Ω, <10% THD
- **Binary Half-Bridge Mode:**
  - **DDX-2062:** 4 x 25 W, 4Ω, <10% THD
  - **DDX-2052:** 4 x 20 W, 4Ω, <10% THD
- SINGLE SUPPLY (+9V to +36V)
- COMPACT SURFACE MOUNT PACKAGE
- HIGH EFFICIENCY, > 90% @ 8Ω, 10%THD
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OVER-VOLTAGE PROTECTION

BENEFITS

- COMPLETE SURFACE MOUNT DESIGN
- POWER SUPPLY SAVINGS

APPLICATIONS

- DIGITAL POWERED SPEAKERS
- PC SOUND CARDS
- CAR AUDIO
- SURROUND SOUND SYSTEMS
- DIGITAL AUDIO COMPONENTS

1.0 GENERAL DESCRIPTION

The DDX-2062/DDX-2052 power devices are monolithic, dual channel H-Bridges that can provide audio power up to:

- 45 watts per channel @10%THD, 8Ω (DDX-2062)
- 40 watts per channel @10%THD, 8Ω (DDX-2052)

at very high efficiency.

Each device contains a logic interface, integrated bridge drivers, high efficiency MOSFET output transistors and protection circuitry. Each device may be used in DDX® Mode as a dual bridge or reconfigured as a single bridge with double the output current capability. Alternatively, in Binary Mode, they may be configured as either a dual bridge or (at lower power output) a quad half-bridge or a combination of both types.

The benefits of the DDX® amplification system are: an all-digital design that eliminates the need for a digital to analog converter (DAC), and the high efficiency operation derived from the use of Apogee's patented damped ternary pulse width modulation (PWM). This approach provides an efficiency advantage over conventional PWM designs and more than three times the efficiency of Class A/B amplifiers with music input signal.

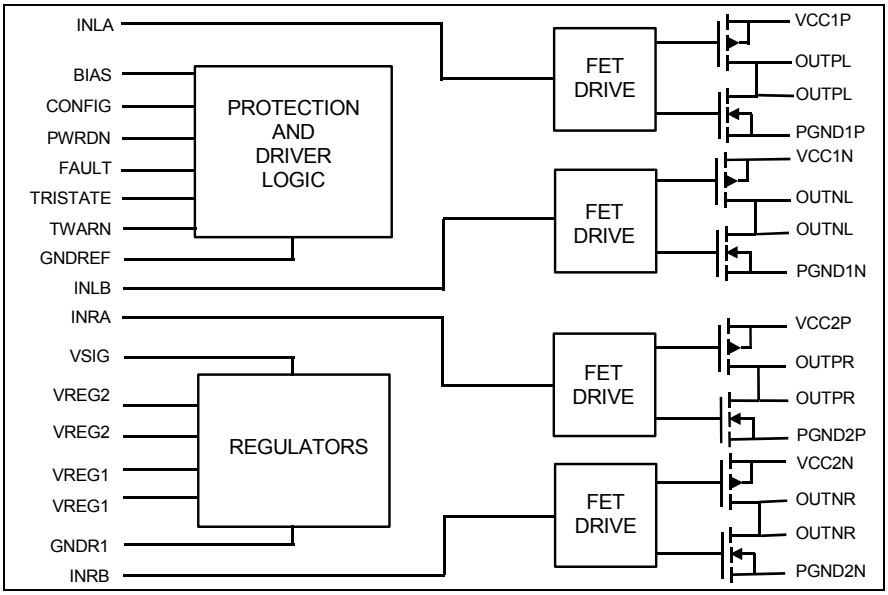


Figure 1. Block Diagram

1.1 Absolute Maximum Ratings [Note 1]

SYMBOL	PARAMETER	VALUE	UNIT
V_{CC}	Power supply voltage	40	V
V_L	Input logic reference	5.5	V
P_{TOT}	Power Dissipation, $T_{heat\text{-}spreader}$ = 25°C [See Figure 4]	50	W
T_j	Operating junction temperature range	0 to +150	°C
T_{stg}	Storage temperature range	-40 to +150	°C

Note 1 - Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.2 Recommended Operating Conditions [Note 2]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Power supply voltage	9.0		36.0	V
V_L	Input logic reference	2.7	3.3	5.0	V
T_A	Ambient Temperature	0		70	°C

Note 2 - Performance not guaranteed beyond recommended operating conditions.

1.3 Thermal Data

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$\theta_{J\text{-}C}$	Thermal resistance junction-case (heat spreader)			2.5	°C/W
$T_{j\text{-}SD}$	Thermal shut-down junction temperature		150		°C
T_{WARN}	Thermal warning temperature		130		°C
T_{hSD}	Thermal shut-down hysteresis		25		°C

1.4 Electrical Characteristics.

[Refer to circuit in Figure 18] Unless otherwise specified, performance is measured using the DDX-8001/DDX-8229 processor family, V_{CC}=28V, VL=3.3V, fsw=384kHz, T_C=25°C, R_L=8Ω.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$P_{O\text{-}DM}$ (DDX® Mono Mode) [Figure 19]	DDX-2062 - Power Per Channel	THD+N <10%, R_L = 4Ω	90			W_{RMS}
		THD+N <1%, R_L = 4Ω	70			
	DDX-2052 - Power Per Channel	THD+N <10%, R_L = 4Ω V_{CC} = 26V	80			
		THD+N <1%, R_L = 4Ω V_{CC} = 26V	62			
$P_{O\text{-}DF}$ (DDX® Full Bridge Mode) [Figure 18]	DDX-2062 – Power Per Channel	THD+N <10%, R_L = 8Ω	45			W_{RMS}
		THD+N <1%, R_L = 8Ω	35			
		THD+N <10%, R_L = 6Ω V_{CC} = 25V	45			W_{RMS}
		THD+N <1%, R_L = 6Ω V_{CC} = 25V	35			
	DDX-2052 - Power Per Channel	THD+N <10%, R_L = 8Ω, V_{CC} = 26V	40			
		THD+N <1%, R_L = 8Ω, V_{CC} = 26V	32			
$P_{O\text{-}Bin}$ (Binary Half-Bridge Mode) [Figure 21]	DDX-2062 - Power Per Channel	THD+N <10%, R_L = 4Ω V_{CC} = 30V	25			W_{RMS}
		THD+N <1%, R_L = 4Ω V_{CC} = 30V	20			
	DDX-2052 - Power Per Channel	THD+N <10%, R_L = 4Ω, V_{CC} = 26V	20			
		THD+N <1%, R_L = 4Ω, V_{CC} = 26V	16			

1.4 Electrical Characteristics.

[Refer to circuit in Figure 18] Unless otherwise specified, performance is measured using the DDX-8001/DDX-8229 processor family, V_{CC}=28V, VL=3.3V, fsw=384kHz, T_C=25°C, R_L=8Ω.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
THD+N	Total Harmonic Distortion + Noise,	Po = 1 Wrms		0.06		%
		Po = 35 Wrms		0.09		
SNR	Signal to Noise Ratio, DDX® Mode	A-Weighted		100		dB
	Signal to Noise Ratio, Binary Half-Bridge Mode			92		
η	Peak Efficiency, DDX® Mode	Po = 2 x 45 W, 8Ω, 10%THD		90		%
	Peak Efficiency, Binary Half-Bridge Mode	Po = 4 x 20 W, 4Ω		87		
I_{SC}	Speaker Output Short-Circuit Protection Limit per Bridge [Note 3]	DDX-2062	3.5	6	8	A
		DDX-2052	3.0	6	8	
$R_{ds\text{-}on}$	Power MOSFET output resistance	I_d = 1A		200	270	mΩ
g_N	Power Nchannel $R_{ds\text{-}on}$ matching	I_d = 1A	95			%
g_P	Power Pchannel $R_{ds\text{-}on}$ matching	I_d = 1A	95			%
I_{dss}	Power Pchannel/Nchannel leakage	V_{CC} = 35 V			50	uA
UVL	Under-voltage Lockout Threshold			7	9	V
I_{PD}	V_{CC} supply current, Power-down	PWRDN = 0		1	3	mA
$I_{CC\text{-}tri}$	V_{CC} supply current, Tri-state	TRISTATE = 0		22		mA
I_{CC}	DDX® mode V_{CC} supply current	2-Channel switching at 384kHz.		75		mA
	Binary mode V_{CC} supply current	4-Channel switching at 384kHz.		84		
t_{on}	Turn-on delay time	Resistive load			100	ns
t_{off}	Turn-off delay time	Resistive load			100	ns
t_r	Rise time	Resistive load			25	ns
t_f	Fall Time	Resistive load			25	ns
V_{IL}	Low logic input voltage: PWRDN, TRISTATE pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V	0.7 0.8 0.85			V
	Low logic input voltage: INLA, INLB, INRA, INRB pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V	1.05 1.35 2.2			
V_{IH}	High logic input voltage: PWRDN, TRISTATE pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V			1.5 1.7 1.85	V
	High logic input voltage: INLA, INLB, INRA, INRB pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V			1.65 1.95 2.8	
I_{fault}	Output Sink Current, FAULT, TWARN pins	Fault Active		1		mA
P_{Wmin}	Minimum output pulse width	No load	70		150	ns

Note 3 – If used in single BTL (Mono Mode) configuration, the device may not be short-circuit protected.

1.5 Logic Truth Table

TRISTATE	InxA	INxB	OUTPx	OUTNx	OUTPUT MODE
0	X	X	OFF	OFF	Hi-Z
1	0	0	GND	GND	DAMPED
1	0	1	GND	VCC	NEGATIVE
1	1	0	VCC	GND	POSITIVE
1	1	1	VCC	VCC	Not Used

2.0 DDX-2062/DDX-2052 Pin Function Description:

2.1 PWM Inputs

	Pin No.	Description
INLA	29	Left A logic input signal
INLB	30	Left B logic input signal
INRA	31	Right A logic input signal
INRB	32	Right B logic input signal

2.2 Control/Miscellaneous

Pin Name	Pin No.	Description
PWRDN	25	Power Down (0=Shutdown, 1= Normal).
TRI-STATE	26	Tri-State (0=All MOSFETS Hi-Z, 1=Normal).
FAULT [Note 4]	27	Fault output indicator; Overcurrent, Overvoltage or Overtemperature (0=Fault, 1=Normal).
TWARN [Note 4]	28	Thermal warning output (0=Warning T_J >= 130°C, 1=Normal).
CONFIG [Note 5]	24	Configuration (0=Normal, 1=Parallel operation for mono).
NC	18	Do not connect.

Note 4: FAULT and TWARN outputs are open-drain
Note 5: Connect CONFIG Pin 24 to VREG1 Pins 21, 22 to implement single bridge (mono mode) operation for high current.

2.3 Power Outputs for DDX® Mode or Binary Full Bridge Mode [Note 6]

Pin Name	Pin No.	Description
OUTPL	16, 17	Left output, positive reference
OUTNL	10, 11	Left output, negative reference
OUTPR	8, 9	Right output, positive reference
OUTNR	2, 3	Right output, negative reference

Note 6: DDX® outputs are bridged. The outputs OUTPx produce signals in phase with the input.

2.4 Power Outputs for Binary Half-Bridge Mode [Note 7]

Pin Name	Pin No.	Description
OUTNR	2, 3	CH4 output, positive reference
OUTPR	8, 9	CH3 output, positive reference
OUTNL	10, 11	CH2 output, positive reference
OUTPL	16, 17	CH1 output, positive reference

Note 7: Half-Bridge Binary Mode outputs are NOT bridged.
All outputs produce signals in phase with the input.

2.5 Power Supplies [Note 8]

Pin Name	Pin No.	Description
VCC [1P, 1N, 2P, 2N]	4, 7, 12, 15	Power
PGND [1P, 1N, 2P, 2N]	5, 6, 13, 14	Power grounds
VREG1	21, 22	Internal regulator voltage requires bypass capacitor.
VREG2	33, 34	Internal regulator voltage requires bypass capacitor.
VSIG	35, 36	Signal Positive supply.
VL	23	Logic reference voltage.
GNDREF	19	Logic reference ground.
GNDS	1	Substrate ground.
GNDR1	20	Internal regulator ground.

Note 8: V_L (Logic Reference Voltage) is recommended to be powered and stable prior to Vcc achieving > 7V to assure proper power up sequence. V_L is recommended to remain powered and stable until after Vcc has decayed below 7V during power removal.

3.0 DDX-2062/DDX-2052 POWER DEVICES

The DDX-2062/DDX-2052 Power Devices are dual channel H-Bridges that can deliver more than 45/40 watts per channel (<10%THD) of audio output power at very high efficiency. They convert both DDX® and binary-controlled PWM signals into audio power at the load. Each includes a logic interface, integrated bridge drivers, high efficiency MOSFET outputs, and thermal and short circuit protection circuitry. In DDX® mode, two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a bridge configuration, according to Apogee's patented damped ternary PWM. In Binary Mode operation, both Full Bridge and Half Bridge Modes are supported. These devices include over-current and thermal protection as well as under-voltage lockout with automatic recovery. A thermal warning status is also provided.

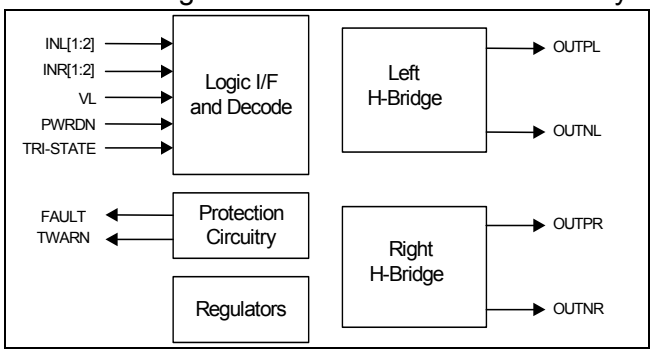


Figure 2 - DDX-2062/2052 Block Diagram, Full- Bridge DDX® or Binary Modes

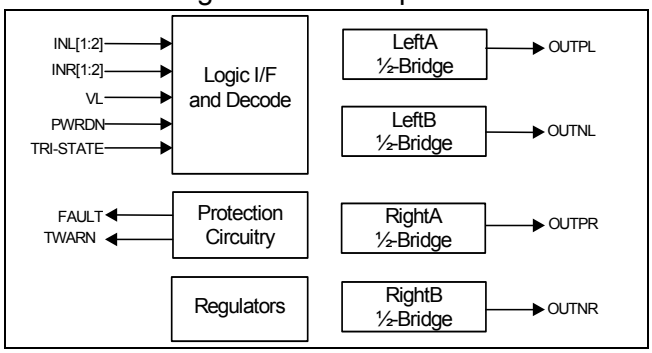


Figure 3 - DDX-2062/2052 Block Diagram, Binary Half-Bridge Mode

3.1 Logic Interface and Decode

The DDX-2062/DDX-2052 power outputs are controlled using one or two logic level timing signals. In order to provide a proper logic interface, the V_L input must operate at the same voltage as the DDX® controller logic supply. VL (Logic Reference Voltage) is recommended to be powered and stable prior to Vcc achieving > 7V to assure proper power up sequence. VL is recommended to remain powered and stable until after Vcc has decayed below 7V during power removal.

3.2 Protection Circuitry

Both the DDX-2062 and the DDX-2052 include protection circuitry for over-current, under-voltage and thermal overload conditions. A thermal warning pin TWARN is activated low (open-drain MOSFET) when the IC temperature exceeds 130°C, in advance of the thermal shutdown protection. When a fault condition is detected (logical OR of over-current and thermal), an internal fault signal acts to immediately disable the output power MOSFETs, placing both H-bridges in a high impedance state. At the same time an open-drain MOSFET connected to the FAULT pin is switched on. There are two possible modes subsequent to activating a fault. The first is a SHUTDOWN mode. With FAULT (pull-up resistor) and TRI-STATE pins independent, an activated fault will disable the device, signaling low at the FAULT output. The device may subsequently be reset to normal operation by toggling the TRI-STATE pin from High to Low to High using an external logic signal.

The second is an AUTOMATIC recovery mode. This is depicted in the application circuit in Figure 18. The FAULT and TRI-STATE pins are shorted together and connected to a time constant circuit comprising of R6 and C17. An activated FAULT will force a reset on the TRI-STATE pin causing normal operation to resume following a delay determined by the time constant of the circuit. If the fault condition is still present, this circuit operation will continue repeating until the fault condition is removed.

An increase in the time constant of the circuit will produce a longer recovery interval. Care must be taken in the overall system design so as not to exceed the protection thresholds under normal operation.

3.3 Power Outputs

The DDX-2062/DDX-2052 power and output pins are duplicated to provide a low impedance path for the device's bridged outputs. All duplicate power, ground and output pins must be connected for proper operation. The PWRDN or TRI-STATE pins should be used to set all MOSFETS to the Hi-Z state during power-up until the logic power supply, V_L, is settled.

3.4 Parallel Output/High Current Operation

When using DDX® Mode output, the DDX-2062/DDX-2052 outputs can be connected in parallel to increase the output current to a load. In this configuration the device can provide over 90/80 Watts into 3Ω/4Ω (see Figure 6). This mode is enabled with the CONFIG pin connected to VREG1 and the inputs combined INLA = INLB, INRA = INRB and outputs combined OUTLA = OUTLB, OUTRA = OUTRB.

3.5 ADDITIONAL INFORMATION

3.6 Output Filter

A passive two-pole low-pass filter is used on the DDX-2062/DDX-2052 power outputs to reconstruct an analog signal. System performance can be significantly affected by the output filter design and choice of components. (See appnote: AN-15, Component Selection for DDX Amplifiers.) A filter design for 6Ω/8Ω loads is shown in the Typical Application Circuit in Figure 18.

3.7 Power Dissipation & Heat Sink Requirements

The power dissipated within the device will depend primarily on the supply voltage, load impedance, and output modulation level.

The surface mount package of the DDX-2062 and DDX-2052 includes an exposed thermal slug on the bottom of the device to provide a direct thermal path from the integrated circuit to the PC Board. Careful consideration must be given to the overall thermal design. See Figure 4 for power derating.

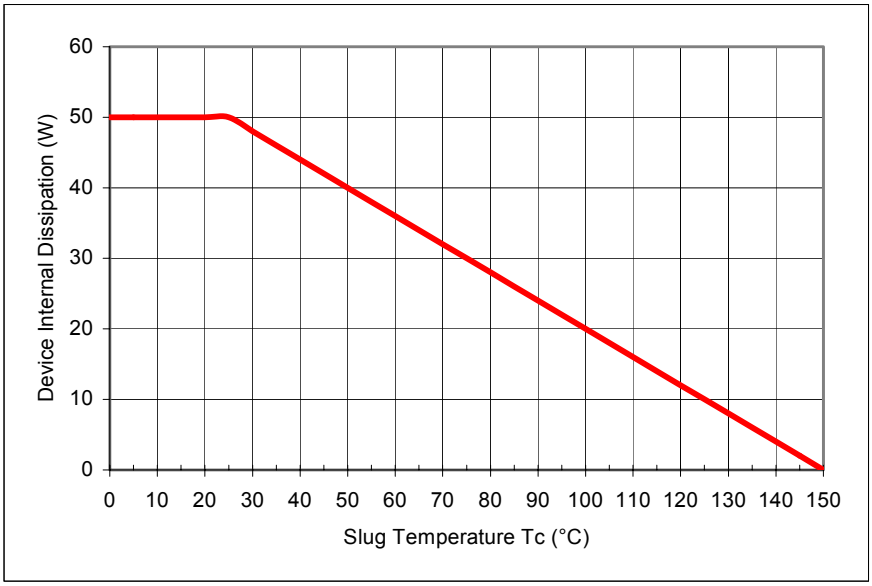


Figure 4 –Power Derating Curve (Typical)

For additional thermal design considerations, see application notes: AN-02, Power Stage Thermal Design for DDX Amps and AN-19, Power Device Thermal Calculator.
For additional design considerations with binary mode operation, see application notes: AN-16, Applying the DDX-8000/DDX-8228 in Binary Mode.

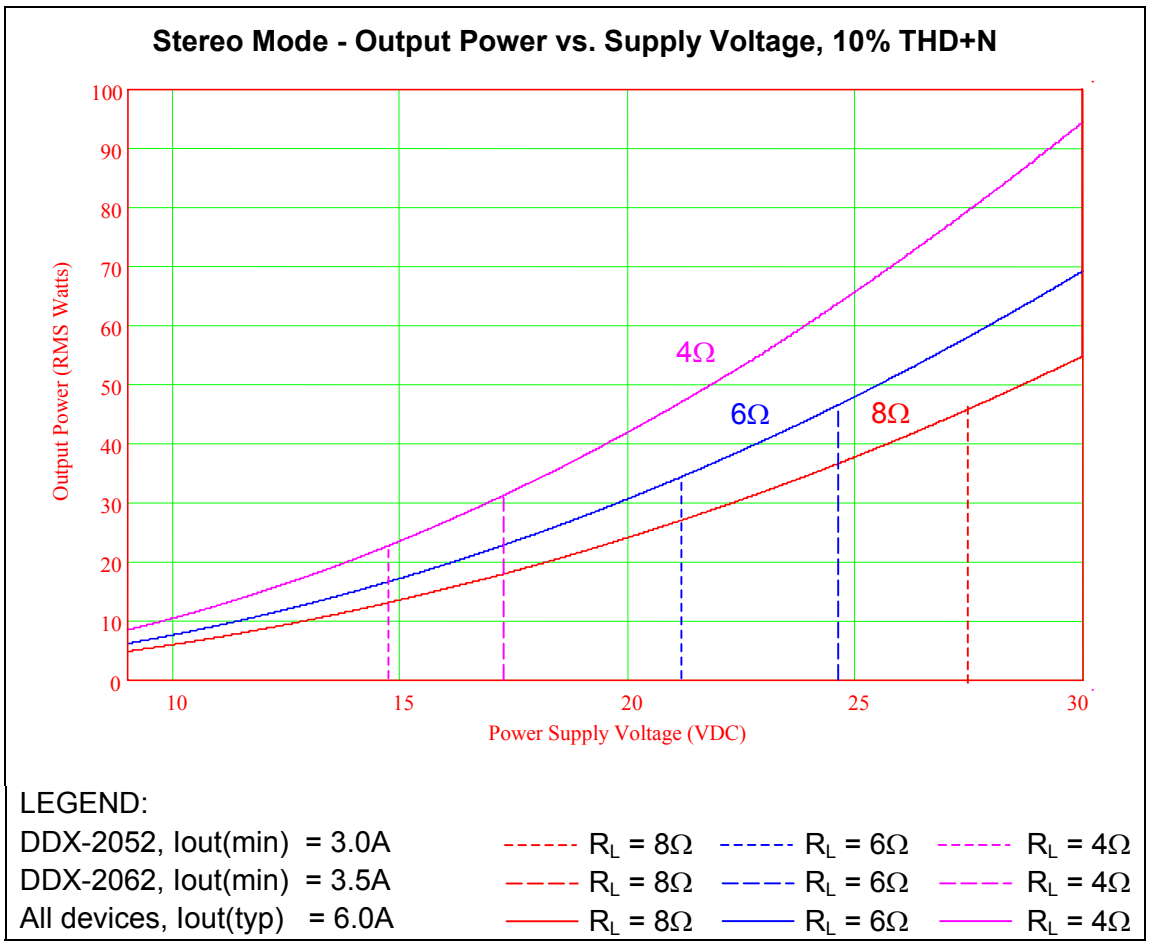


Figure 5. Stereo Bridge Output Power vs. Supply Voltage, 10% THD+N.

Figure 5shows the 10% THD output power as a function of Power Supply Voltage for 4, 6, and 8 Ohm loads in either DDX® Mode or Binary Full Bridge Mode. Output power is constrained for higher impedance loads by the maximum voltage limit of the DDX-2062/DDX-2052 ICs and by the over-current protection limit for lower impedance loads. The minimum threshold for the over-current protection circuit is 3.5/3.0A (at 25 ºC) but the typical threshold is 6.0A. Solid curves depict typical output power capability of each device. Dotted and dashed curves depict the output power capability constrained to the minimum current specification of the DDX-2052 and DDX-2062 respectively. The output power curves assume proper thermal management of the power device's internal dissipation. See Figure 4.

NOTE: Output power at <1% THD is approximately 22% lower.

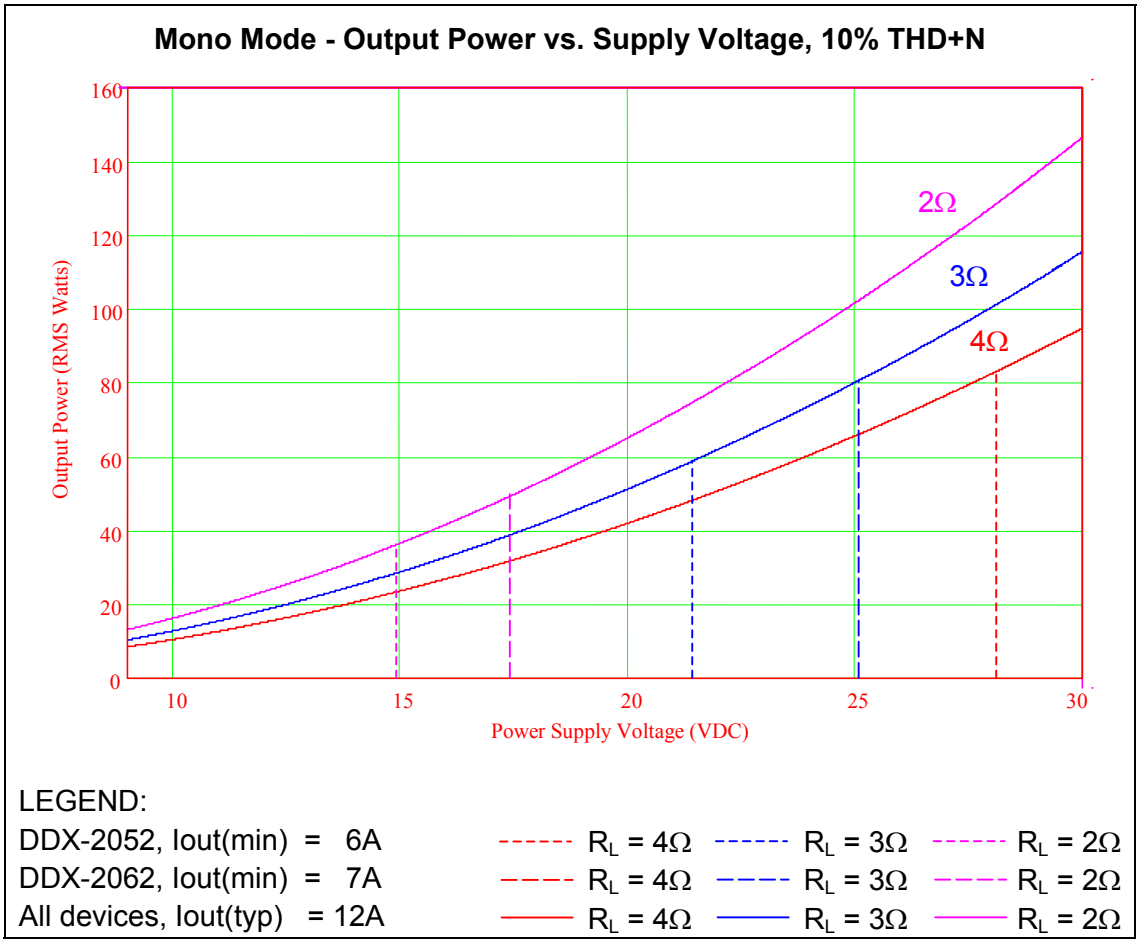


Figure 6. Mono Bridge, DDX® Mode Only, Output Power vs Supply Voltage at 10% THD+N.

Figure 6 depicts the mono mode 10% THD output power as a function of power supply voltages for loads of 2, 3, and 4 Ohms. The same current limit observations from Figure 5 apply, except output current is 9A/7A minimum, 12A typical in mono bridge configuration. Solid curves depict typical performance and dotted and dashed curves depict the minimum current limit for the DDX-2052 and DDX-2062 respectively. Again, the output power curves assume proper thermal management of the power device's internal dissipation.

NOTE: Output power at <1% THD is approximately 22% lower.

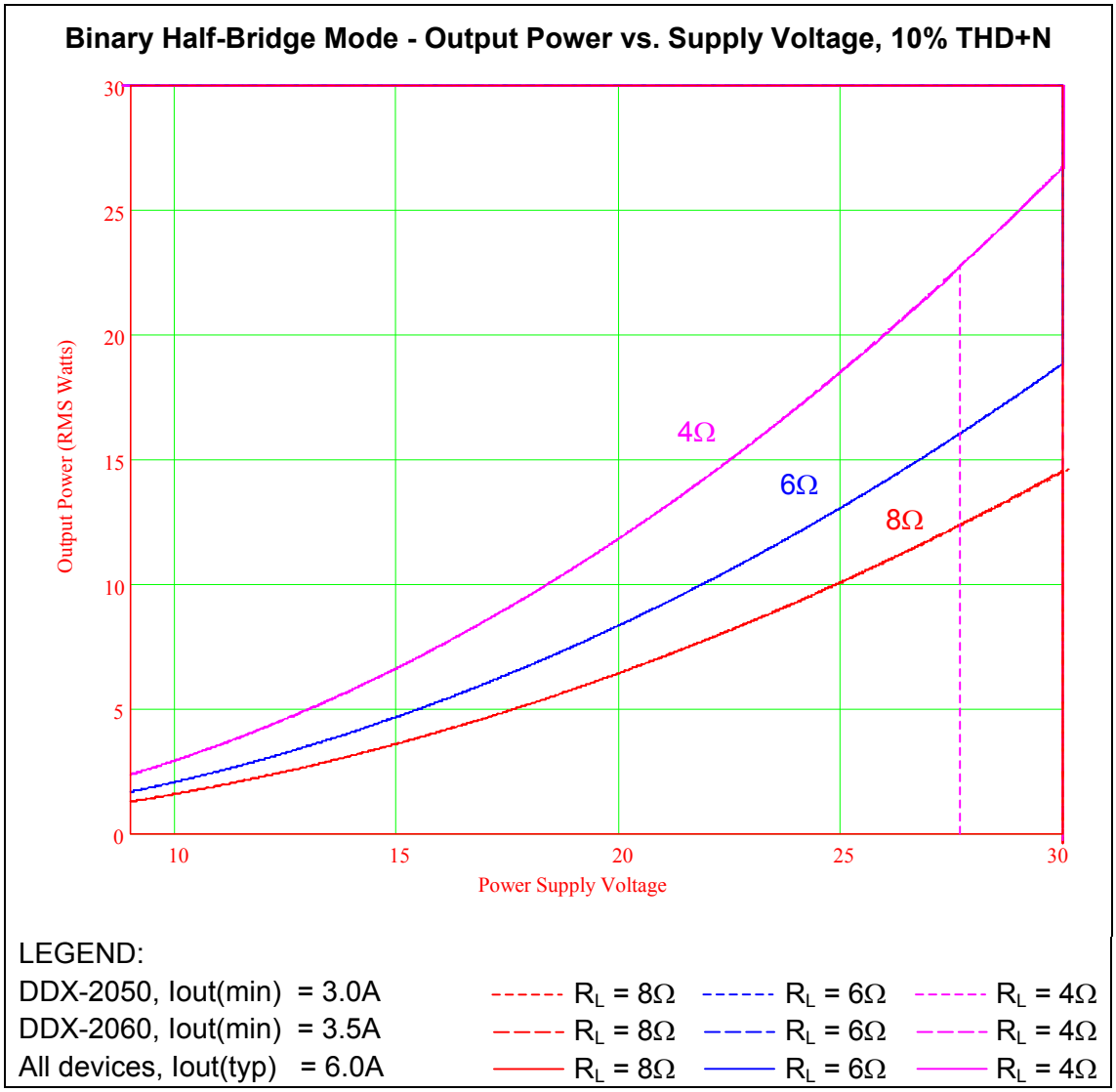


Figure 7. Half-Bridge Binary Mode Output Power vs Supply Voltage at 10% THD+N.
(NOTE: Curves taken at f = 1 kHz and using a 330uF blocking capacitor.)

Figure 7 depicts the 10% THD output power as a function of power supply voltages for loads of 4, 6, and 8 Ohms when the DDX-2062/DDX-2052s are operated in a half-bridge Binary Mode. Solid curves depict typical performance and dotted and dashed curves depict the minimum current limit for the DDX-2052 and DDX-2062 respectively. Once again, the output power curves assume proper thermal management of the power device's internal dissipation.

NOTE: Output power at <1% THD is approximately 22% lower.

3.8 Power Supply and Control Sequencing.

Figure 8 shows the recommended power-up and power-down sequencing. The "time zero" reference point is taken where Vcc crosses the Undervoltage Lockout threshold.

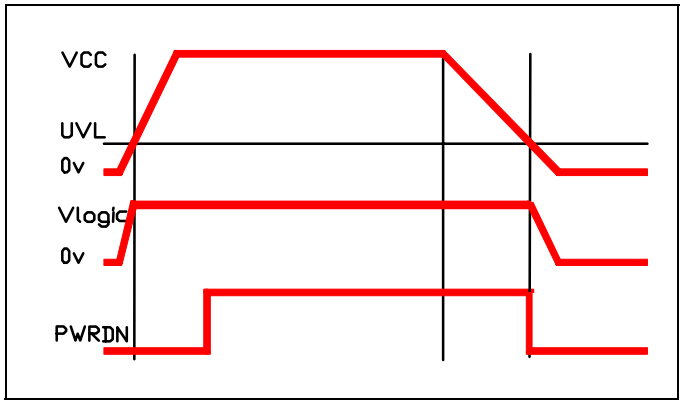
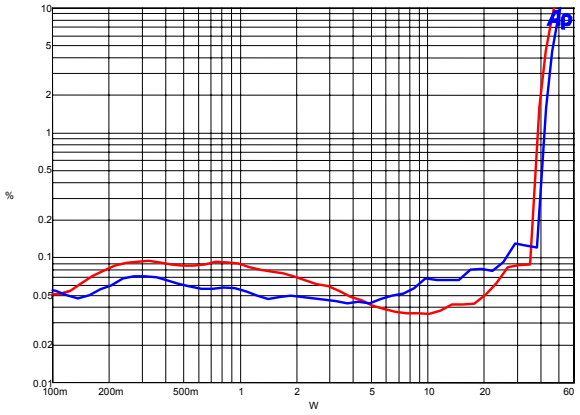
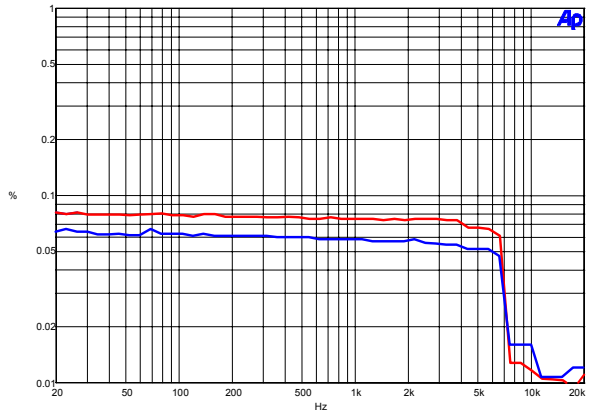


Figure 8 – Recommended Power-Up & Power-Down Sequence

3.9 Typical Stereo Mode Performance Characteristics.



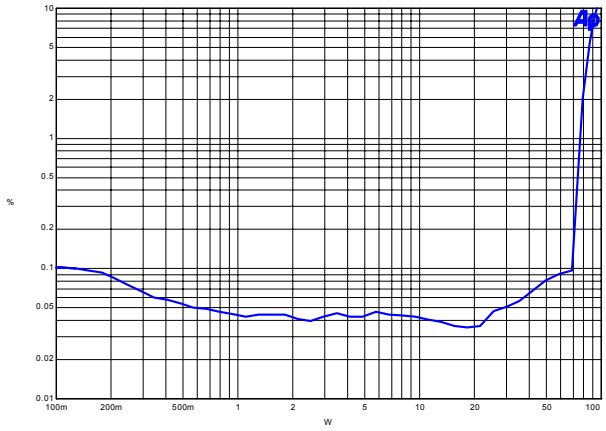


V_{CC} = 28VDC, R_L = 8Ω V_{CC} = 26VDC, R_L = 6Ω V_{CC} = 28VDC, R_L = 8Ω V_{CC} = 26VDC, R_L = 6Ω

Figure 9. THD+N vs. Output Power @ 1kHz

Figure 10. THD+N vs. Frequency

3.10 Typical Mono Mode Performance Characteristics, Vcc = 28VDC, RL = 4Ω.



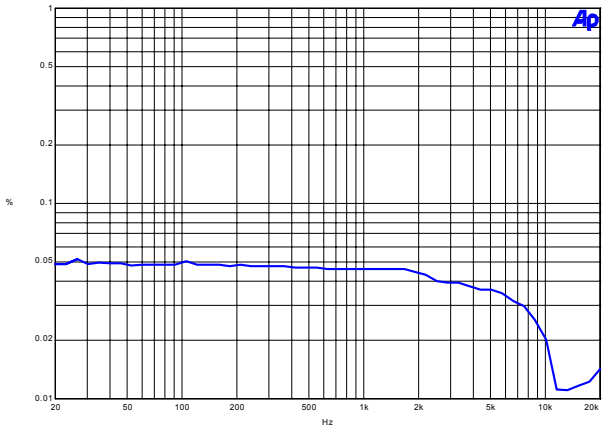
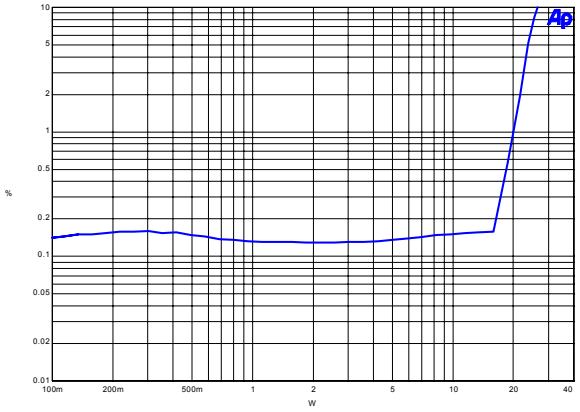


Figure 11. THD+N vs. Output Power @ 1kHz

Figure 12. THD+N vs. Frequency

3.11 Typical Binary Half-Bridge Mode Performance Characteristics, V_{CC} = 28 VDC, R_L - 4Ω.



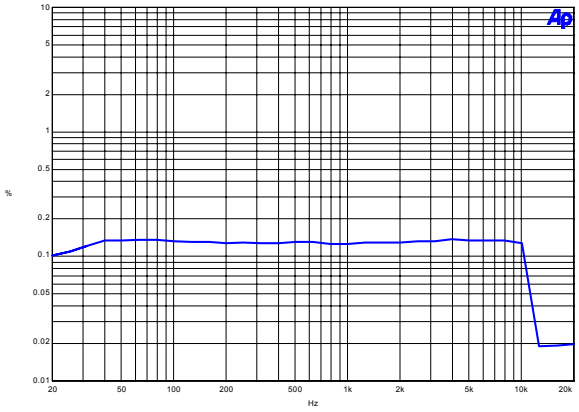


Figure 13. THD+N vs. Output Power @ 1kHz

Figure 14. THD+N vs. Frequency

3.12 Typical DDX-Mode Performance Characteristics at V_{CC} = 28V, 8Ω Load, <1% THD+N.

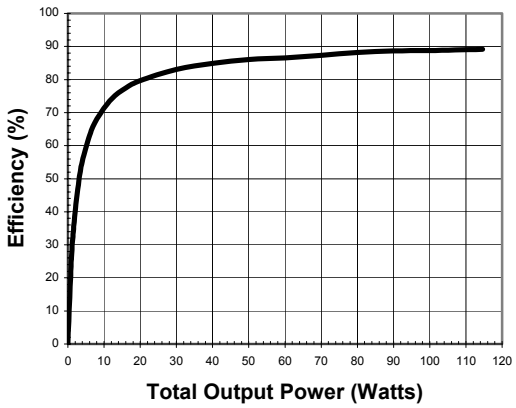


Figure 15. Typical Efficiency vs. PowerEfficiency

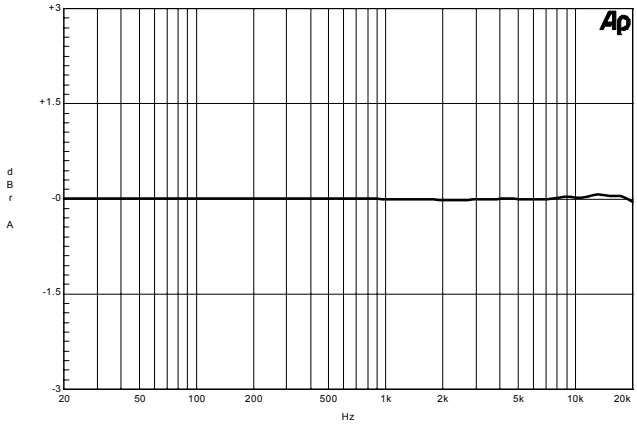


Figure 16. Typical Frequency Response

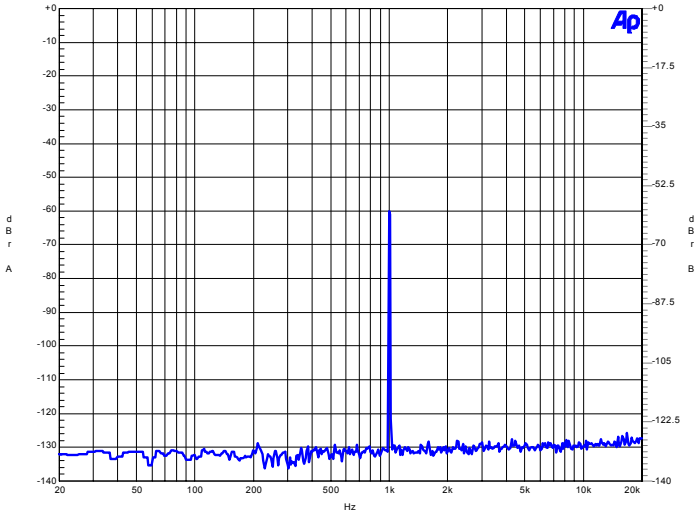


Figure 17. Typical FFT @ -60 dB

4.0 APPLICATION REFERENCE DESIGN.

Apogee can provide reference designs for most applications.
Contact Apogee Technical Support for more information.

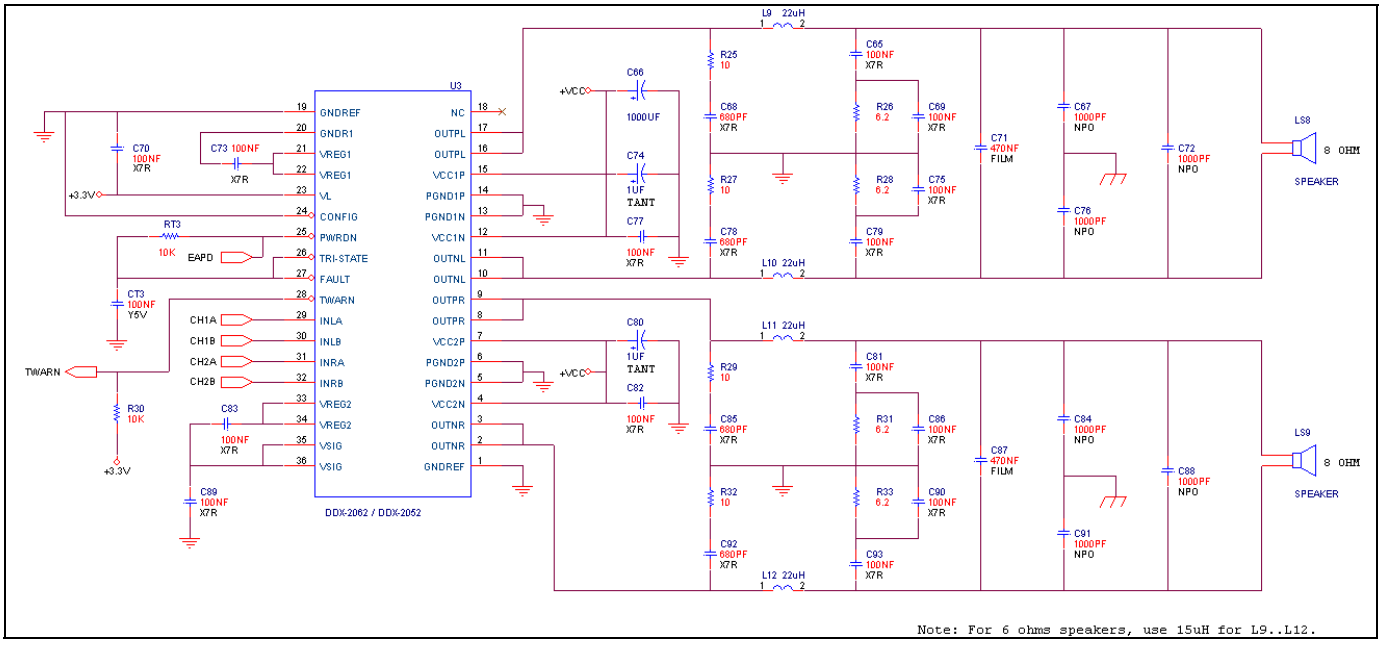


Figure 18. DDX® Stereo Mode Audio Application Circuit

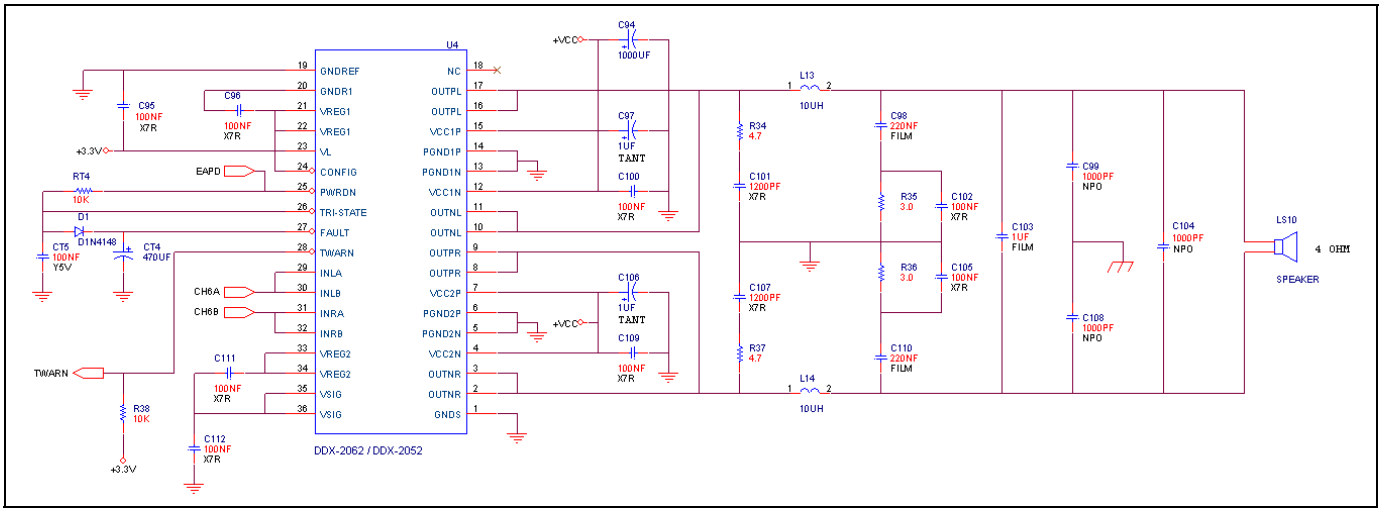


Figure 19. DDX® Mono Mode Audio Application Circuit

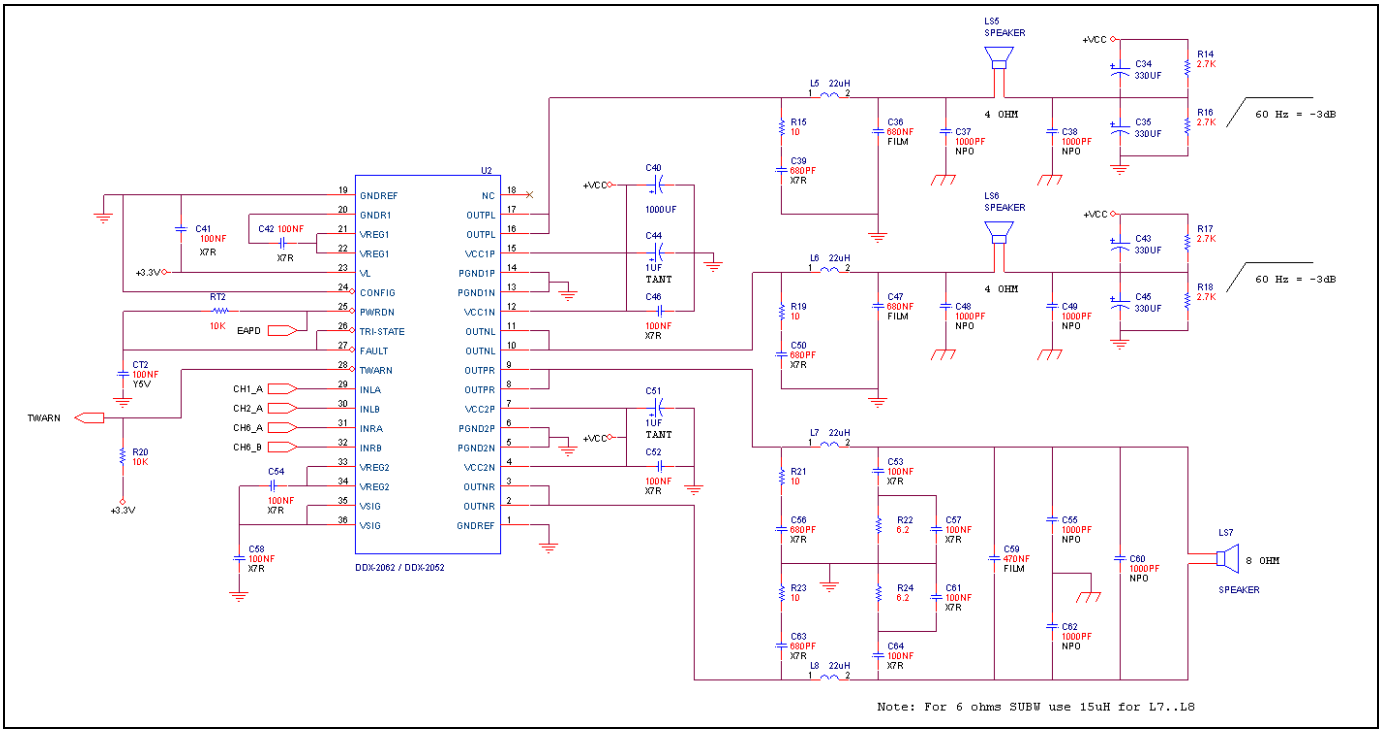


Figure 20 Binary Mode, 2.1 Channel Audio Application Circuit (See Note 9)

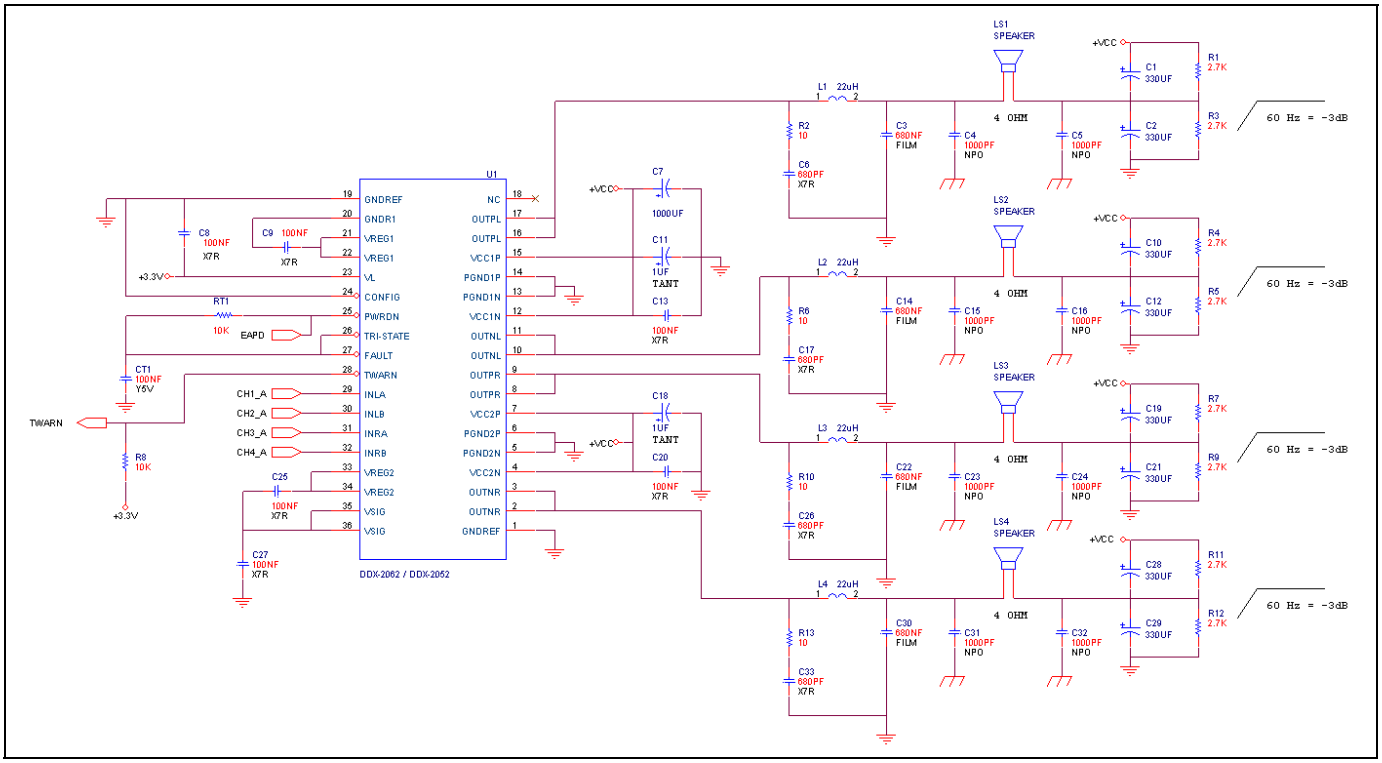


Figure 21. DDX® ½-Bridge Mode Audio Application Circuit (See Note 9)

Note 9: Channel mappings in Binary mode schematics apply to DDX-8229 PWM output channels.

Specifications are subject to change without notice.

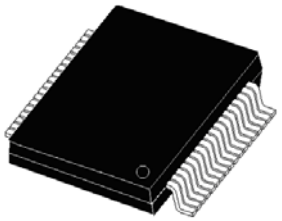
5.0 PACKAGE INFORMATION

5.1 Package Outline Drawing

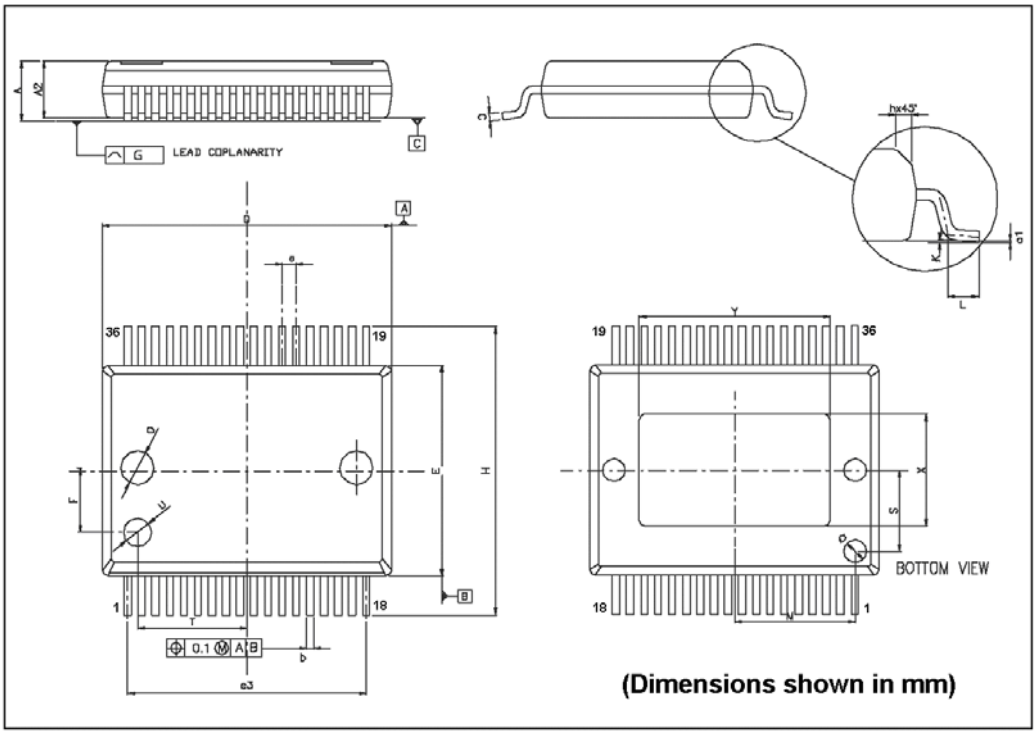
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.15		2.47	0.084		0.097
A2	2.15		2.40	0.084		0.094
a1	0		0.075	0		0.003
b	0.18		0.36	0.007		0.014
c	0.23		0.32	0.009		0.012
D (1)	10.10		10.50	0.398		0.413
E (1)	7.4		7.6	0.291		0.299
e		0.50			0.020	
e3		8.50			0.035	
F		2.3			0.090	
G			0.10			0.004
G1			0.06			0.002
H	10.10		10.50	0.398		0.413
h			0.40			0.016
L	0.55		0.85	0.022		0.033
M		4.3			0.169	
N	10° (max)					
O		1.2			0.047	
Q		0.8			0.031	
S		2.9			0.114	
T		3.65			0.144	
U		1.0			0.039	
X	4.10		4.70	0.161		0.185
Y	6.50		7.10	0.256		0.279

(1) "D and E" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
(2) No intrusion allowed inwards the leads.
(3) Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side

OUTLINE AND MECHANICAL DATA



PowerSSO-36 (slug-down)



Specifications are subject to change without notice.

5.2 Marking Configuration

Packages with Date Code (YWW) = 514 & after





LEGEND:

LLLWXTFP	Traceability Coding
COO	Country Of Origin
Y	Assembly Year
WW	Assembly Week
e3	Pb-Free (RoHS Compliant) (no symbol if not Pb-Free)

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